References

[1] Altenbernd, P. "On the false path problem in hard real-time programs". *Proceedings of the Euromicro Workshop on Real-Time Systems.* Los Alamitos: IEEE Computer Society Press, June 1996.

[2] Altenbernd, P.; and Milczewski, R. "Description of timing problems using Petri nets for level-independent timing verification". *Proceedings of the ACM/SIGDA Workshop on Timing Issues in the Specification and Synthesis of Digital Systems.* 1993.

[3] Amroun, A.; and Bolton, M. "Synthesis fo controllers from Petri net descriptions and application of Ella". *In:* L.J.M. Claesen (ed.), *Formal VLSI specification and synthesis*. North-Holland: Elsevier Science Publishers, 1990, pp. 291-308.

[4] Ancilotti, P.; Butazzo, G.C.; Di Natale, M.; and Bizzarri, M. "The MORIS control system". *Proceedings of the Euromicro Workshop on Real-Time Systems.* Los Alamitos: IEEE Computer Society Press, June 1996, pp. 77-82.

[5] Aubury, M.; Page, I.; Randall, G.; Saul, J.; and Watts, R. "The Handel-C language reference guide". Computing Laboratory, Oxford University, UK: 1996.

[6] Audsley, N.; and Burns, A. "Real-time system scheduling". Technical Report YCS 134, University of York - Department of Computer Science: 1990.

[7] Audsley, N.; and Burns, A. "Deadline monotonic scheduling". Technical Report YCS 146, University of York - Department of Computer Science: 1991.

[8] Barros, E. "Hardware/software partitioning using UNITY". Ph.D. Thesis, Fakultat fur Informatik der Eberhard-Karls-Universitat zu Tubingen, 1993.

[9] Barros, E.; and Rosenstiel, W. "A method for hardware-software partitioning". *Proceedings of the Annual European Computer Conference - Compeuro 92.* Los Alamitos: IEEE, 1992, pp. 580-585.

[10] Barros, E.; Rosenstiel, W.; and Xiong, X. "Method for partitioning UNITY language in hardware and software". *Proceedings of the European Design Automation Conference.* Los Alamitos: IEEE, September 1994, pp. 220-225.

[11] Barros, E.; and Sampaio, A. "Towards provably correct hardware/software partitioning using occam". *Proceedings of the 3rd International Workshop on Hardware/Software Codesign.* Los Alamitos: IEEE, September 1994, pp. 210-217.

[12] Benders, L.P.M. "Analysis of real-time embedded systems for co-design". *Proceedings of the 6th IEEE International Workshop on Rapid System Prototyping.* Los Alamitos: IEEE, June 1995, pp. 26-32.

[13] Benner, T.; Ernst, R.; and Oesterling, A. "Scalable performance scheduling for hardware-software cosynthesis". *Proceedings of the European Design Automation Conference with EURO-VHDL.* Los Alamitos: IEEE, September 1995, pp. 164-169.

[14] Benveniste, A.; and Berry, G. "The synchronous approach to reactive and real-time systems". *Proceedings of the IEEE*, **79**(9): 1270-1282, 1991.

[15] Bilinski, K.; Adamski, M.; Saul, J.M.; and Dagless, E.L. "Parallel controller synthesis from a Petri net specification". *Proceedings of the European Design Automation Conference - EURO-DAC'94.* 1994, pp. 96-101.

[16] Borriello, G.; Chou, P.; and Ortega, R. "Embedded system co-design". *In:* G. DeMicheli, and M. Sami (eds.), *Hardware/software co-design*. Dordrecht: Kluwer Academic Publishers, 1996, pp. 243-264.

[17] Buchenrieder, K.; Sedlmeier, A.; and Veith, C. "HW/SW Co-design with PRAMs using CODES". *Proceedings of the 11th IFIP WG10.2 International Conference on Computer Hardware Description Languages and their Applications - CHDL'93.* Amsterdam: Elsevier Science Publishers, 1993, pp. 65-78.

[18] Buchenrieder, K.; Sedlmeier, A.; and Veith, C. "Industrial hw/sw co-design". *In:* J. Rozenblit, and K. Buchenrieder (eds.), *Hardware/software co-design*. New York: IEEE Press, 1995, pp. 378-393.

[19] Burns, A.; and Fohler, G. "Incorporating flexibility into offline scheduling for hard real-time systems". Technical Report RR-03-91, School of Computer Science, Technische Universität Wien: 1991.

[20] Burns, A.; and Wellings, A. , *Real-time systems and their programming languages*. Padstow: Addison-Wesley Publishers Ltd. 1990.

[21] Burns, A.; and Wellings, A.J. "HRT-HOOD: A structured design method for hard real-time systems". *Real-Time Systems*, **6**(1): 73-114, 1994.

[22] Casavant, T.L.; and Kuhl, J.G. "Taxonomy of scheduling in general-purpose distributed computing systems". *IEEE Transactions on Software Engineering*, **14**(2): 141-154, 1988.

[23] Cavalcante, S.V.; and Kinniment, D.J. "The use of Petri nets for hardware/software codesign". Technical Report EE/0594/M1, Department of Electrical and Electronic Engineering, University of Newcastle upon Tyne, UK: 1994.

[24] Cavalcante, S.V.; and Kinniment, D.J. "Petri-net based codesign system for real-time applications". *Proceedings of the IEE Computing and Control Division Colloquium on Partitioning in Hardware - Software Codesigns.* Stevenage: IEE, February 1995, pp. 7/1-7/3.

[25] Cavalcante, S.V.; and Kinniment, D.J. "Time Wizard: a design and assessment tool for real-time applications". *Proceedings of the Euromicro Workshop on Real-Time Systems.* Los Alamitos: IEEE Computer Society Press, June 1996, pp. 22-27.

[26] Cavalcante, S.V. "A hardware-software codesign environment for real-time embedded applications". *In:* C. Muller-Schloer, F. Geerinckx, B. Stanford-Smith, and R. van Riet (eds.), *Embedded microprocessor systems*. Amsterdam: IOS Press, 1996, pp. 253-262.

[27] Chang, W.T.; Kalavade, A.; and Lee, E.A. "Effective heterogeneous design and co-simulation". *In:* G. DeMicheli, and M. Sami (eds.), *Hardware/software co-design*. Dordrecht: Kluwer Academic Publishers, 1996, pp. 187-212.

[28] Chiodo, M.; Giusto, P.; Hsieh, H.C.; Jurecska, A.; Lavagno, L.; and SangiovanniVincentelli, A. "A formal specification model for hardware-software codesign". Technical Report ERL-93-48, University of California, Berkeley, USA: 1993.

[29] Chiodo, M.; Giusto, P.; Hsieh, H.C.; Jurecska, A.; Lavagno, L.; and SangiovanniVincentelli, A. "Synthesis of mixed software-hardware implementations from CFSM specifications". Technical Report ERL-93-49, University of California, Berkeley, USA: 1993.

[30] Chiodo, M.; Giusto, P.; Jurecska, A.; Hsieh, H.C.; SangiovanniVincentelli, A.; and Lavagno, L. "Hardware-software codesign of embedded systems". *IEEE Micro*, **14**(4): 26-36, 1994.

[31] Chou, P.; and Borriello, G. "Software scheduling in the co-synthesis of reactive real-time systems". *Proceedings of the 31st Design Automation Conference.* Piscataway: IEEE, June 1994, pp. 1-4.

[32] Chou, P.; Walkup, E.A.; and Borriello, G. "Scheduling for reactive real-time systems". *IEEE Micro*, **14**: 37-47, 1994.

[33] DAmbrosio, J.G.; and Hu, X. "Configuration-level hardware/software partitioning for real-time embedded systems". *Proceedings of the 3rd International Workshop on Hardware/Software Codesign.* Los Alamitos: IEEE, September 1994, pp. 34-41.

[34] DeMicheli, G. "Computer-aided hardware-software codesign". *IEEE Micro*, **14**(4): 10-16, 1994.

[35] DeMicheli, G. "Hardware/software co-design: application domains and design technologies". *In:* G. DeMicheli, and M. Sami (eds.), *Hardware/software co-design*. Dordrecht: Kluwer Academic Publishers, 1996, pp. 1-28.

[36] DeMicheli, G.; Ku, D.; Mailhot, F.; and Truong, T. "The Olympus synthesis system for digital design". Center for Integrated Systems, Stanford University, Stanford, USA: 1990.

[37] Eles, P.; Kuchcinski, K.; Peng, Z.; and Minea, M. "Compiling VHDL into a high-level synthesis design representation". *Proceedings of the European Design Automation Conference - EURO-VHDL '92.* Los Alamitos: IEEE Computer Society, September 1992, pp. 604-609.

[38] Eles, P.; Kuchcinski, K.; Peng, Z.; and Minea, M. "Synthesis of VHDL concurrent processes". *Proceedings of the European Design Automation Conference.* Los Alamitos: IEEE, September 1994, pp. 540-545.

[39] Eles, P.; Peng, Z.; and Doboli, A. "VHDL system-level specification and partitioning in a hardware/software co-synthesis environment". *Proceedings of the 3rd International Workshop on Hardware/Software Codesign.* Los Alamitos: IEEE, September 1994, pp. 49-55.

[40] Eles, P.; Peng, Z.; Kuchcinski, K.; and Doboli, A. "Hardware/software partitioning of VHDL system specifications". *Proceedings of the European Design Automation Conference with EURO-VHDL'96.* Los Alamitos: IEEE, September 1996, pp. 434-439.

[41] Ernst, R.; Henkel, J.; and Benner, T. "Hardware/software cosynthesis for microcontrollers". *IEEE Design & Test of Computers*, **10**(4): 64-75, 1993.

[42] Ernst, R.; Henkel, J.; Benner, T.; Ye, W.; Holtmann, U.; Herrmann, D.; and Trawny, M. "COSYMA environment for hardware/software cosynthesis of small embedded systems". *Microprocessors and Microsystems*, **20**(3): 159-166, 1996.

[43] Estrin, G. "A methodology for design of digital systems - supported by SARA at the age of one". *Proceedings of the National Computer Conference.* 1978, pp. 313-324.

[44] Garey, M.R.; and Johnson, D.S. "Complexity Results for Multiprocessor Scheduling under Resource Constraints". *SIAM Journal on Computing*, **4**(4): 397-411, 1975.

[45] Garey, M.R.; and Johnson, D.S. , *Computers and intractability: a guide to the theory of NP-completeness*. San Francisco, USA: Freeman, 1979.

[46] Genrich, H.J.; and Lautenbach, K. "System modelling with high-level Petri nets". *Theoretical Computer Science*, **13**: 109-136, 1981.

[47] Ghezzi, C.; Mandrioli, D.; Morasca, S.; and Pezze, M. "A general way to put time in Petri nets". *Proceedings of the 5th International Workshop on Software Specification and Design.* ACM, May 1989, pp. 60-67.

[48] Ghezzi, C.; Mandrioli, D.; Morasca, S.; and Pezze, M. "A unified high-level Petri net formalism for time-critical systems". *IEEE Transactions on Software Engineering*, **17**(2): 160-172, 1991.

[49] Gong, J.; Gajski, D.D.; and Narayan, S. "Software estimation using a generic-processor model". *Proceedings of the European Design and Test Conference, ED&TC.* Los Alamitos: IEEE, March 1995, pp. 498-502.

[50] Gopinath, P.; and Gupta, R. "Applying compiler techiniques to scheduling in real-time systems". *Proceedings of the 11th Real-Time Systems Symposium.* December 1990, pp. 247-256.

[51] Gupta, R.K. "Co-synthesis of hardware and software for digital systems". Ph.D. Thesis, Department of Electrical Engineering, Stanford University, Stanford, USA, 1993.

[52] Gupta, R.K.; Coelho, C.N.; and DeMicheli, G. "Synthesis and simulation of digital systems containing interacting hardware and software components". *Proceedings of the 29th ACM/IEEE Design Automation Conference.* Piscataway: IEEE, June 1992, pp. 225-230.

[53] Gupta, R.K.; and DeMicheli, G. "System level synthesis using re-programmable components". *Proceedings of the European Design Automation Conference.* Piscataway: IEEE, March 1992, pp. 2-7.

[54] Gupta, R.K.; and DeMicheli, G. "Co-synthesis approach to embedded system design automation". *Design Automation for Embedded Systems*, **1**(1-2): 69-120, 1996.

[55] Gupta, R.K.; and Micheli, G.D. "Hardware-software cosynthesis for digital systems". *IEEE Design & Test of Computers*, **10**(3): 29-41, 1993.

[56] Gupta, R.K.; Micheli, G.D.; and Coelho, C.N. "Program implementation schemes for hardware-software systems". *Computer*, **27**(1): 48-55, 1994.

[57] Gusfield, D. "Bounds for naive multiple machine scheduling with release times and deadlines". *Journal of Algorithms*, **5**(1): 1-6, 1984.

[58] Herrmann, D.; Henkel, J.; and Ernst, R. "An approach to the adaptation of estimated cost parameters in the COSYMA system". *Proceedings of the 3rd International Workshop on Hardware/Software Codesign.* Los Alamitos: IEEE, September 1994, pp. 100-107.

[59] Hoare, C.A.R. "Communicating sequential processes". *Communications of the ACM*, **21**(8): 666-667, 1978.

[60] Hou, J.; and Wolf, W. "Process partitioning for distributed embedded systems". *Proceedings of the 4th International Workshop on Hardware/Software Codesign, Codes/CASHE'96.* Los Alamitos: IEEE, March 1996, pp. 70-76.

[61] Hu, X.; DAmbrosio, J.G.; Murray, B.T.; and Tang, D.L. "Codesign of architectures for automotive powertrain modules". *IEEE Micro*, **14**(4): 17-25, 1994.

[62] Huber, P.; Jensen, K.; and Shapiro, R.M. "Hierarchies in coloured Petri nets". *In:* K. Jensen, and G. Rozenberg (eds.). Berlin: Springer-Verlag, 1991, pp. 215-243.

[63] INMOS Ltd. "The transputer applications notebook: architecture and software". Redwood Burn Ltd. 1989.

[64] Ivy Team "SystemSpecs 2.1 - Getting Started". Ivy Team, Switzerland: 1993.

[65] Ivy Team "SystemSpecs 2.1 - Reference Manual". Ivy Team, Switzerland: 1993.

[66] Jensen, K. Brauer, W.; Reisig, W.; and Rozenberg, G. (eds), *Coloured Petri nets*. Springer-Verlag, 1987.

[67] Jensen, K. "Coloured Petri nets: a high-level language for system design and analysis". *In:* G. Rozenberg (ed.), *Advances in Petri Nets 1990*. Berlin: Springer-Verlag, 1990, pp. 342-416.

[68] Kalavade, A.; and Lee, E.A. "A hardware-software codesign methodology for DSP applications". *IEEE Design & Test of Computers*, **10**(3): 16-28, 1993.

[69] Kappos, E.; and Kinniment, D.J. "Application-specific processor architectures for embedded control: Case studies". *Microprocessors and Microsystems*, **20**(4): 225-232, 1996.

[70] Kappos, E.; Kinniment, D.J.; Acarnley, P.P.; and Jack, A.G. "The design of an integrated circuit controller for brushless DC drives". *Proceedings of the Fourth International Conference on Power Electronics and Variable- Speed Drives, London, Engl, 17-19 Jul 1990, (Conf. code 13545).* IEE, Michael Faraday House, Stevenage, Engl. 1990, pp. 336-341.

[71] Keen, C.D.; and Lakos, C.A. "Information systems modelling using LOOPN++, an object Petri net scheme". *Proceedings of the 4th International Working Conference on Dynamic Modelling and Information Systems.* 1994, pp. 31-52.

[72] Klein, M.H.; Ralya, T.; Pollak, B.; Obenza, R.; and Harbour, M.G. , *A practitioner's handbook for real-time analysis: guide to Rate Monotonic Analysis for real-time systems*. Norwell: Kluwer Academic Publishers, 1993.

[73] Koch, G.; Kebschull, U.; and Rosenstiel, W. "Prototyping environment for hardware/software codesign in the COBRA project". *Proceedings of the 3rd*

International Workshop on Hardware/Software Codesign. Los Alamitos: IEEE, September 1994, pp. 10-16.

[74] Kopetz, H. "Should responsive systems be event-triggered or time-triggered ?". Technical Report Second Year Report, ESPRIT Basic Research Project 6362-PDCS 2: Predictably Dependable Computing Systems, Second Year Report, 1994.

[75] Kramer, J.; Magee, J.; Sloman, M.S.; and Lister, A.M. "CONIC: an integrated approach to distributed computer control systems". *IEE Proceedings (Part E)*, **180**(1): 1-10, 1983.

[76] Ku, D.; and DeMicheli, G. "HardwareC: a language for hardware design". Technical Report CSL-TR-90-419, Computer System Laboratory, Stanford University, Stanford, USA: 1990.

[77] Ku, D.C.; and DeMicheli, G. "Relative scheduling under timing constraints: Algorithms for high- level synthesis of digital circuits". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **11**(6): 696-718, 1992.

[78] Lagnese, E.D.; and Thomas, D.E. "Architectural partitioning for system level design". *Proceedings of the 26th ACM/IEEE Design Automation Conference.* June 1989, pp. 62-67.

[79] Lakos, C.A.; and Keen, C.D. "Simulation with object-oriented Petri nets". *Proceedings of the Australian Software Engineering Conference.* July 1991, pp. 14p.

[80] Lawrence, A.; Kay, A.; Luk, W.; Nomura, T.; and Page, I. "Using reconfigurable hardware to speed up product development and performance". Computing Laboratory, Oxford University, UK: 1994.

[81] Leung, J.Y.T.; and Whitehead, J. "On the complexity of fixed-priority scheduling of periodic, real-time tasks". *Performance Evaluation*, **2**(4): 237-250, 1982.

[82] Leveson, N.G.; and Stolzy, J.L. "Safety analysis using petri nets". *IEEE Transactions on Software Engineering*, **SE-13**(3): 386-397, 1987.

[83] Levi, S.; and Agrawala, A.K. , *Real-time system design*. New York: McGraw-Hill Publishing Co. 1990.

[84] Lew, A. , *Computer science: a mathematical introduction*. London: Prentice Hall International, 1984.

[85] Liu, C.L.; and Layland, J.W. "Scheduling Algorithms for Multiprogramming in a Hard-Real-Time Environment". *Journal of the ACM*, **20**(1): 46-61, 1973.

[86] Maciel, P.; and Barros, E. "Captura de requerimentos temporais usando redes de Petri para o particionamento de hardware/software". *Proceedings of the I Brazilian Workshop on Hardware/Software Codesign.* Recife: Departamento de Informatica - UFPE, March 1996, pp. 383-396.

[87] Mahony, B.P.; and Hayes, I.J. "A case-study in timed refinement: A mine pump". *IEEE Transactions on Software Engineering*, **18**(9): 817-826, 1992.

[88] Malik, S.; Wolf, W.; Wolfe, A.; Li, Y.; and Yen, T.Y. "Performance analysis of embedded systems". *In:* G. DeMicheli, and M. Sami (eds.), *Hardware/software co-design*. Dordrecht: Kluwer Academic Publishers, 1996, pp. 45-74.

[89] Marsan, M.A. "Stochastic Petri nets: an elementary introduction". *In:* G. Rozenberg (ed.), *Advances in Petri nets*. Springer-Verlag, 1989, pp. 1-29.

[90] Marsan, M.A.; Balbo, G.; Chiola, G.; Conte, G.; Donatelli, S.; and Franceschinis, G. "Introduction to generalized stochastic Petri nets". *Microelectronics and Reliability*, **31**(4): 699-725, 1991.

[91] Minea, M. "A VHDL compiler for a high-level synthesis system". Technical Report LiTH-IDA-R-93-23, Department of Computer and Information Science, Linköping University, Sweden: 1993.

[92] Mok, A.K. "Design of real-time programming systems based on process models". *Proceedings of the Real-Time Systems Symposium.* New York: IEEE, December 1984, pp. 5-17.

[93] Murata, T. "Petri nets: properties, analysis and applications". *Proceedings of the IEEE*, **77**(4): 541-580, 1989.

[94] Page, I. "Executable specification is the key to hardware/software codesign". *New Electronics*, **27**(13): 27-28, 1994.

[95] Page, I. "Automatic design and implementation of microprocessors". *Proceedings of the WoTUG-17.* Amsterdam: IOS Press, April 1994, pp. 190-204.

[96] Page, I. "Constructing hardware-software systems from a single description". *Journal of VLSI Signal Processing*, **12**(1): 87-107, 1996.

[97] Page, I. "Reconfigurable processor architectures". *Microprocessors and Microsystems*, **20**(3): 185-196, 1996.

[98] Page, I. "Video motion tracking using Harp and Handel: a case study". *Proceedings of the 7th Annual Advanced PLD and FPGA Conference.* London: Miller Freeman, May 1997.

[99] Peng, Z.; and Kuchcinski, K. "An algorithm for partitioning of application specific systems". *Proceedings of the European Design Automation Conference.* Los Alamitos: IEEE, March 1993, pp. 316-321.

[100] Pezze, M.; and Ghezzi, C. "Cabernet: a customizable environment for the specification and analysis of real-time systems". Dipartimento di Elettronica e dell'Informazione, Politecnico de Milano: 1992.

[101] Poledna, S. "Tolerating sensor timing faults in highly responsive hard real-time systems". *IEEE Transactions on Computers*, **44**(2): 181-191, 1995.

[102] Rammig, F. "Modelling aspects of system level design". *Proceedings of the European Design Automation Conference - Euro-DAC'93.* June 1993, pp. 534-539.

[103] Reinersten, D.G. "Whodunit ? The search for the new-product killers". McKinsey & Company: 1983.

[104] Reisig, W. , *Petri nets - an introduction*. Springer-Verlag, 1985.

[105] Sha, L.; Lehoczky, J.P.; and Rajkumar, R. "Task scheduling in distributed real-time systems". *Proceedings of the International Conference on Industrial Electronics, Control, and Instrumentation - IECON '87.* New York: IEEE, November 1987, pp. 909-916.

[106] Sha, L.; Rajkumar, R.; and Lehoczky, J.P. "Priority inheritance protocols: an approach to real-time synchronization". *IEEE Transactions on Software Engineering*, **39**(9): 1175-1185, 1990.

[107] Shepard, T.; and Gagne, J.A.M. "A pre-run-time scheduling algorithm for hard real-time systems". *IEEE Transactions on Software Engineering*, **17**(7): 669-677, 1991.

[108] Shepard, T.; and Gagne, M. "A model of the F18 mission computer software for pre-run-time scheduling". *Proceedings of the 10th International Conference on Distributed Computing Systems - ICDCS-10.* Piscataway: IEEE, May 1990, pp. 62-69.

[109] Shirazi, B.A.; Hurson, A.R.; and Kavi, K.M. (eds), *Scheduling and load balancing in parallel and distributed systems*. IEEE Press, 1995.

[110] Shrivastava, S.K.; Mancini, L.V.; and Randell, B. "Duality of fault-tolerant system structures". *Software - Practice and Experience*, **23**(7): 773-798, 1993.

[111] Sibertin-Blanc, C. "Cooperative objects for the conceptual modelling of organizational information systems". *Proceedings of the IFIP TC8 Working Conference on The Object Oriented Approach in Information Systems.* October 1991, pp. 28-31.

[112] Silva, S. "Cabernet user manual". Dipartimento di Elettronica e dell'Informazione, Politecnico de Milano: 1994.

[113] Sprunt, B.; Sha, L.; and Lehoczky, J. "Aperiodic task scheduling for hard-real-time systems". *Real-Time Systems*, **1**(1): 27-60, 1989.

[114] Strosnider, J.K.; Lehoczky, J.P.; and Sha, L. "Deferrable server algorithm for enhanced aperiodic responsiveness in hard real-time environments". *IEEE Transactions on Computers*, **44**(1): 73-91, 1995.

[115] Tindell, K.W.; Burns, A.; and Wellings, A.J. "Allocating hard real-time tasks: an NP-Hard problem made easy". *Real-Time Systems*, **4**(2): 145-165, 1992.

[116] Wendling, M.; and Rosenstiel, W. "Hardware environment for prototyping and partitioning based on multiple FPGAs". *Proceedings of the European Design Automation Conference.* Los Alamitos: IEEE, September 1994, pp. 77-82.

[117] Wolf, W.H. "Hardware-software co-design of embedded systems". *Proceedings of the IEEE*, **82**(7): 967-989, 1994.

[118] Xu, J. "Multiprocessor scheduling of processes with release times, deadlines, precedence, and exclusion relations". *IEEE Transactions on Software Engineering*, **19**(2): 139-154, 1993.

[119] Xu, J.; and Parnas, D.L. "Scheduling processes with release times, deadlines, precedence, and exclusion relations". *IEEE Transactions on Software Engineering*, **16**(3): 360-369, 1990.

[120] Xu, J.; and Parnas, D.L. "On satisfying timing constraints in hard-real-time systems". *IEEE Transactions on Software Engineering*, **19**(1): 70-86, 1993.

[121] Yakovlev, A.; Semenov, A.; Koelmans, A.M.; and Kinniment, D.J. "Petri nets and asynchronous circuit design". *Proceedings of the 1996 IEE Colloquium on Design and Test of Asynchronous Systems, London, UK, Feb 28 1996, (Conf. code 45663).* IEE, Stevenage, Engl, 1996, pp. 8/1-8/6.

[122] Ye, W.; Ernst, R.; Benner, T.; and Henkel, J. "Fast timing analysis for hardware-software co-synthesis". *Proceedings of the IEEE International Conference on Computer Design: VLSI in Computers & Processors.* Piscataway: IEEE, October 1993, pp. 452-457.

[123] Young, S.J. , *Real time languages: design and development*. Chichester: Ellis Horwood, 1982.