10. SINGLE-SUPPLY PUSH-PULL AMPLIFIER

The push-pull amplifier circuit as discussed in section-9 requires a dual power supply. It can be tailored to operate on a single supply as illustrated in Figure 10.1. In this case the load is isolated with a capacitor. The capacitor is selected on the basis of the lowest possible 3-dB frequency. For example, for an audio amplifier, the 3-dB frequency can be selected as 20 Hz. The biasing circuit is designed with the understanding that the dc voltage at the junction between the two diodes is 0.5 $V_{CC}$ with respect to the reference (ground). If we assume that the diode voltage drop is exactly equal to the base-to-emitter voltage drop of each transistor, then the voltage at the emitter terminals of the two transistors is also 0.5 $V_{CC}$. In other words, at the Q-point, the capacitor $C_L$ on the output side is charged to a voltage of 0.5 $V_{CC}$.

The two resistors in series with the diodes form the biasing circuits for the two current mirrors. The biasing current through each diode should be large enough to keep the diodes ON for all input voltages. Simply stated, we must ensure that the maximum negative peak current through each diode must be less than the dc bias current. We will satisfy this condition by selecting $R$ on the basis of maximum output voltage.

![Figure 10.1: Single supply push-pull amplifier](image-url)
When Q1 (NPN transistor) conducts, the output voltage is positive and the capacitor $C_L$ is charged to 0.5 $V_{CC}$. At the mid-band frequency, the capacitor impedance is so small that it can be neglected and time-varying (ac) component of the voltage at the emitter end of Q1 is exactly equal to the output voltage. When the output voltage is at its maximum we can assume that the only current through $R$ is the base current of Q1. Let $V_{O\ (MAX)}$ be the output voltage. Then the maximum collector current (assuming $\alpha = 1$) is

$$I_{C\ (MAX)} = I_{O\ (MAX)} = \frac{V_{O\ (MAX)}}{R_L}$$

(10.1)

The corresponding maximum base current is

$$I_{B\ (MAX)} = \frac{I_{C\ (MAX)}}{\beta}$$

(10.2)

We can select $R$ on the basis of maximum base current. That is

$$R = \frac{0.5\ V_{CC} - V_{BE\cdot Q1} - V_{O\ (MAX)}}{I_{B\ (MAX)}}$$

(10.3)

The above equation yields the maximum value of $R$ that we can select. If we select a value for $R$ less than that given by the above equation, then the current through $R$ would be greater than $I_{B\ (MAX)}$. This does not pose any threat because the excess current can flow through D1.
The maximum possible collector current can be obtained from the intersection of the ac load line with the current axis as shown in Figure 10.2. Note that the dc load line is vertically upward and it passes through 0.5 \( V_{CC} \). The ac load line also passes through 0.5 \( V_{CC} \) and intersects the current axis at

\[
I_{ACM} = \frac{V_{CC}}{2R_L}
\]  

(10.4)

This is the maximum current that can never be realized in a practical design because of the saturation voltage of the transistor. However, we can use it to predict the theoretically possible maximum efficiency of the amplifier.

Let us assume that \( I_{ACM} \) is the maximum collector current. Then the maximum load current is also \( I_{ACM} \). The theoretically possible maximum value of the average power output is

\[
P_{O,AVG(MAX)} = \frac{1}{2} I_{ACM}^2 R_L = \frac{V_{CC}^2}{8R_L}
\]  

(10.5)

In order to obtain the theoretically possible maximum efficiency, let us neglect the power loss in the biasing circuit. The NPN transistor Q1 is ON only during the positive cycle of the output voltage. During the negative cycle of the output voltage, the PNP transistor Q2 is ON and the capacitor \( C_L \) supplies power to Q2. The power supplied by the source during the negative half-cycle is therefore zero.

The maximum possible average power supplied to the transistors by the supply is then

\[
P_{S,AVG(MAX)} = \frac{1}{\pi} I_{ACM} V_{CC} = \frac{V_{CC}^2}{2\pi R_L}
\]  

(10.6)

Thus, the maximum possible efficiency that we can theoretically obtained is

\[
\eta = \frac{P_{O,AVG(MAX)}}{P_{S,AVG(MAX)}} = \frac{\pi}{4} = 0.7854 \quad \text{or} \quad 78.54\%
\]

This is the same result we obtained earlier. As we know it, such a high efficiency is beyond the reach of a class-B amplifier especially when we account for the losses in the biasing circuit.
When we subtract the power output (10.5) from the power input (10.6), we obtain the total power dissipated by the two transistors in the circuit. Thus, the power dissipated by each transistor is one-half as much. That is,

$$P_T = \frac{1}{2} \left( \frac{1}{\pi} I_{ACM} V_{CC} - \frac{1}{2} I_{ACM}^2 R_L \right)$$  \hspace{1cm} (10.7)

To obtain the maximum power dissipated by each transistor, we have to differentiate the above expression with respect to $I_{ACM}$, set it equal to zero, and solve for $I_{ACM}$. After performing these operations, we obtain

$$I_{ACM} = \frac{V_{CC}}{\pi R_L}$$  \hspace{1cm} (10.8)

When we substitute (10.8) in (10.7), we obtain the maximum power dissipated by each transistor as

$$P_{T(MAX)} = \frac{V_{CC}^2}{4 \pi^2 R_L}$$  \hspace{1cm} (10.9)

To be on the safe side, we will use (10.9) as the criterion for the selection of the transistor.

Thus far, we have not used any safety factor in our design. The safety factor is usually employed to ensure that the transistors will behave as expected and the amplifier will deliver the required power without much distortion. As far as I am concerned, I always try to use a safety factor of 10% to 25%. In the example that follows, let us use a safety factor of 15%.

**Example 10.1: Designing of a Single-Supply Push-Pull Amplifier**

Design the single-supply push-pull amplifier of the type shown in Figure 10.1 to deliver 2 W to an 8-Ω speaker over the frequency range of 20 Hz and 20 kHz. A 24-V dc power supply is available for this amplifier. Use a matched pair of PNP and NPN transistors each having $\beta = 100$ and $|V_{BE}| = 0.7$ V. Assume that the transistors are also used as diodes in the circuit.

**Solution:**

The required power output is 2 W. In order to avoid the operation in the nonlinear regions, let us use a safety factor of 15%. Thus, we shall design the circuit to deliver an average power of $2 \times 1.15 = 2.3$ W to the 8-Ω speaker.
The effective (rms) value of the time-varying current through the 8-Ω speaker is

\[ I_{O(rms)} = \sqrt{\frac{2.3}{8}} = 0.536 \text{ A} \]

Thus, the maximum (peak) value of the current in the speaker is

\[ I_{O(MAX)} = \sqrt{2} \times 0.5362 = 0.758 \text{ A} \]

Consequently, the peak (maximum) value of the output voltage is

\[ V_{O(MAX)} = I_{O(MAX)} R_L = 0.758 \times 8 = 6.064 \text{ V} \]

As mentioned earlier, we select \( R \) on the basis of maximum output voltage and the maximum base current. The maximum base current is

\[ I_{B(MAX)} = \frac{I_{O(MAX)}}{\beta + 1} = 7.505 \text{ mA} \]

Note that we have used \((\beta + 1)\) in the above equation because \( I_{O(MAX)} \) is the emitter current. You could have used \( \beta \) to compute an approximate value of the base current as long as \( \beta \geq 100 \).

The biasing resistor \( R \) can now be computed, from (10.3), as

\[ R = \frac{(12 - 0.7 - 6.064) \text{ V}}{7.505 \text{ mA}} = 697.67 \text{ Ω} \]

**Let us select \( R = 680 \text{ Ω} \).**

The dc biasing current through the diodes is

\[ I_D = \frac{24 - 0.7 - 0.7}{2 \times 680} = 16.618 \text{ mA} \]

The average collector current is

\[ I_{C(AVG)} = \frac{1}{\pi} I_{O(MAX)} = \frac{0.758}{\pi} = 241.128 \text{ mA} \]

Thus, the average current supplied by the 24-V dc source is

\[ I_S = I_D + I_{C(AVG)} = 16.618 + 241.128 = 257.746 \text{ mA} \]

Hence, the dc power supplied by the 24-V source is

\[ P_S = (24 \text{ V})(257.746 \text{ mA}) = 6.186 \text{ W} \]

Since we are using the transistors as diodes, \( n=1 \). The ac resistance of each diode is

\[ r_d = \frac{25 \text{ mV}}{16.618 \text{ mA}} = 1.5 \text{ Ω} \]
We can now draw the ac equivalent circuit as shown in Figure 10.3a where \((\beta+1)R_L\) is the equivalent load resistance as viewed from the base circuit of Q1. Figure 10.3a shows the exact equivalent circuit. Since \(r_d\) is so small in comparison with \(R\), we can assume that each diode acts as a short circuit for the ac signal. The approximate equivalent circuit of Figure 10.3b is drawn without the resistances of the two diodes.

It is evident from Figure 10.3b that the input resistance is simply the parallel combination of the three resistors. That is,

\[
R_{in} = R \parallel R \parallel (\beta+1) R_L = 680 \parallel 680 \parallel (8 \times 10^1) = 239.3 \ \Omega.
\]

If the computed value of the input resistance is small and the loading effect is a problem, the driver stage can simply be an emitter follower with very low output resistance and relatively high input resistance. We can even use a Darlington transistor in the emitter follower configuration in order to increase the input resistance.

\[\text{(a)}\] \hspace{2cm} \text{(b)}

\[\text{Figure 10.3: (a) Exact ac equivalent circuit and (b) approximate counterpart}\]
From the approximate equivalent circuit of Figure 10.3b it is clear that the maximum value of the input voltage is the same as that of the output voltage. That is
\[ V_{in(MAX)} = V_{O(MAX)} = 6.064 \text{ V} \]

Keep in mind that we have replaced each diode with a short circuit. Thus, the maximum value of the input current is
\[ I_{in(MAX)} = \frac{V_{in(MAX)}}{R_{in}} = \frac{6.064}{239.3} = 25.341 \text{ mA} \]

Hence, the current gain:
\[ A_I = \frac{I_{O(MAX)}}{I_{in(MAX)}} = \frac{758 \text{ mA}}{25.341 \text{ mA}} = 29.9 \]

Note that the voltage gain is approximately equal to unity. Therefore, the power gain is 29.9.

Since we are planning for a power output of 2 W and the total power input is 6.186 W, the overall efficiency is 32.33%. We can increase the efficiency by decreasing the dc voltage supply or by increasing the power output requirement.

The maximum power that each transistor would dissipate is
\[ P_{T(MAX)} = \frac{V_{cc}^2}{4 \pi^2 R_L} = \frac{24^2}{4 \pi^2 \times 8} = 1.82 \text{ W} \]

The transistor should be selected on the basis of 1.82 W of power dissipation at the operating temperature.

**Selection of C_L:**

Since the lowest 3-dB frequency is given as 20 Hz, the capacitor size can be computed as
\[ C_L = \frac{1}{2 \pi f_c R_L} = \frac{1}{2 \pi \times 20 \times 8} = 994.7 \text{ } \mu\text{F} \]

**Let us use C_L = 1000 \mu F. In fact, we can also use C_1 as 1000 \mu F.**

The design is now complete. Now is the time to verify the design by actually building the circuit and testing it. Have fun doing so!
The circuit has been analyzed using PSpice. The program is given on the next page. The program name is **PPSS.CIR** (Push-Pull Single Supply). The output current (through the capacitor \(C_L\)) and the input current (through \(C_1\)) are sketched. The peak value of the output current is 732.7 mA and that of the input current is 24.93 mA. We computed these currents as 758 mA and 25.34 mA, respectively. The current gain is \(\frac{732.7}{24.93} = 29.4\). This is very close to the theoretically obtain value of 29.9 for the current gain. PSpice lets you to plot the average power output by using the command \(\text{AVG}(I(R_L)^{\ast}I(R_L)^{\ast}8)\). Read the average value at the end of 3rd or 4th period. It is around 2.17 W or so. Since we only need 2 watts as the output, the design seems to have met our requirements.

**Push-Pull Single-Supply, PPSS.CIR**

```
VCC 1 0 DC 24
VIN 9 0 SIN(0 6.06 10000)
RL 3 0 8
R1 1 8 680
R2 5 0 680
CL 2 3 1000UF
C1 9 7 1000UF
Q1 1 8 2 NPN1
Q2 0 5 2 PNP2
D1 8 7 DIOD
D2 7 5 DIOD
.MODEL DIOD D
.MODEL NPN1 NPN BF=100 IS=1E-14
.MODEL PNP2 PNP BF=100 IS=1E-14
.TRAN 0.1US 400US 0 0.1US
.PROBE
.END
```