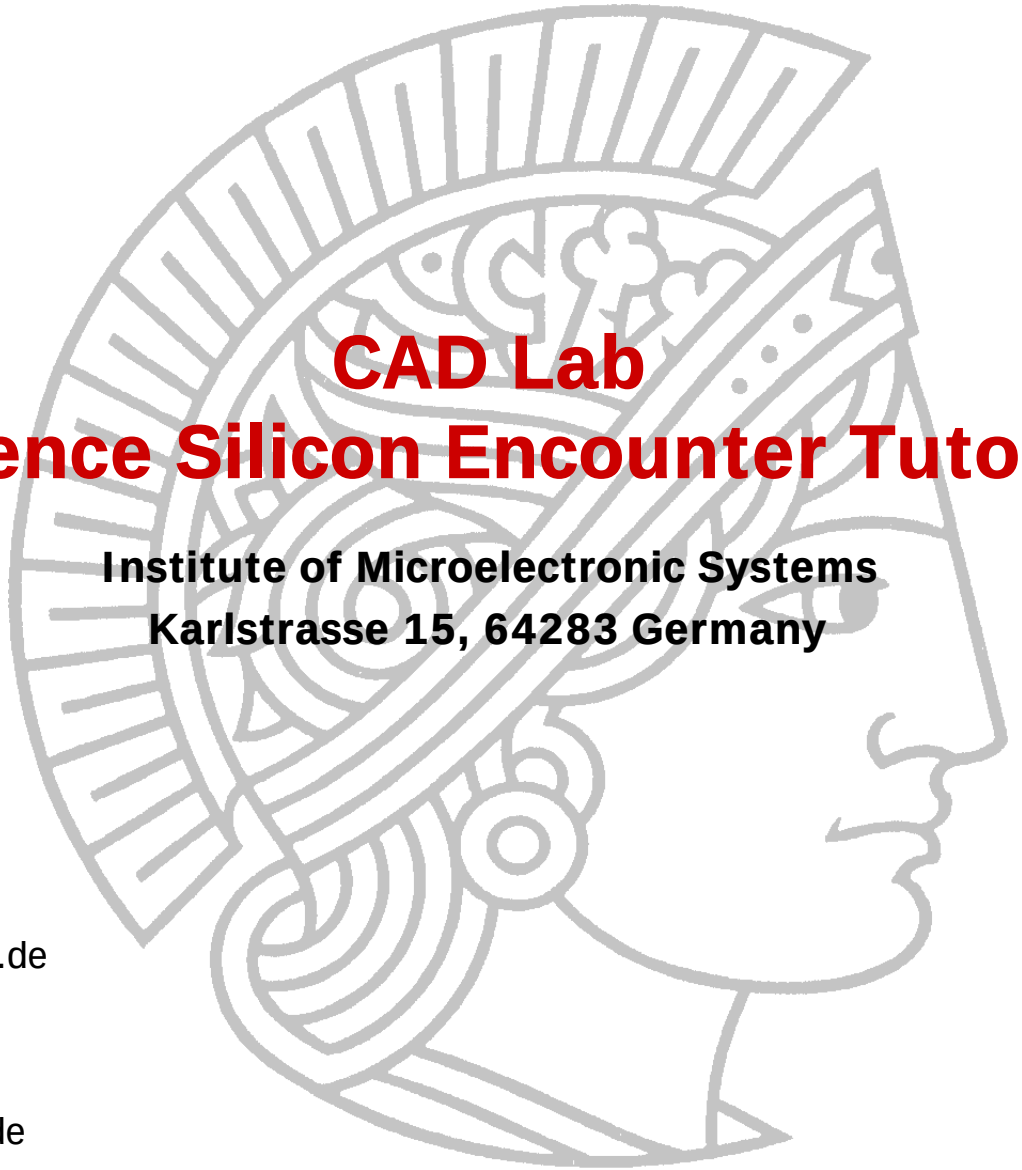

CAD Lab
Cadence Silicon Encounter Tutorial

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Cadence Silicon Encounter & Basic Steps

File Preparation

- The verilog structural code file obtained from Synopsys tool
- Modify the structural verilog file by adding IO pad cells.
- Create IO Assignment file

Place & Route

- Floorplanning
- Create Power Ring
- Cell Area and IO Place
- Global Route

Verify and Save

- Verifiy the design result
- Save design in GDSII file

- Cadence Silicon Encounter
  - A tool to create the circuit layout of the digital circuit automatically using Standard-Cell technology.
- Staggered IO Pad Cell names using UMC standard-cell technology:
  - VVDD = Power pad.
  - VVSS = Ground pad.
  - C3I40 = Input Pad.
  - C3O10 = Output Pad.
  - C18C32 = Clock Pad.
- Inline IO Pad Cell names using UMC standard-cell technology:
  - WVVDD = Power pad.
  - WVVSS = Ground pad.
  - WC3I40 = Input Pad.
  - WC3O10 = Output Pad.
  - WC18C32 = Clock Pad.

Modify the file by adding IO Pad with Staggered IO

```
module mux_4to1_4bit_PAD ( inport0_IP, inport1_IP, inport2_IP, inport3_IP, outport_OP, control_IP);
  input [3:0] inport0_IP;
  input [3:0] inport1_IP;
  input [3:0] inport2_IP;
  input [3:0] inport3_IP;
  output [3:0] outport_OP;
  input [1:0] control_IP;

  wire   n18, n19, n20, n21, n22, n23, n24, n25, n26, n27, n28, n29, n30, n31;
  wire [3:0] inport0, inport1, inport2, inport3, outport;
  wire [1:0] control;

  CORNER SE_CORNER; CORNER SW_CORNER; CORNER NE_CORNER; CORNER NW_CORNER;
  VVDD VDD ();
  VVSS VSS ();

  C3I40 IN0_0 ( .PAD(inport0_IP[0]),  .DI(inport0[0]));
  C3I40 IN0_1 ( .PAD(inport0_IP[1]),  .DI(inport0[1]));
  C3I40 IN0_2 ( .PAD(inport0_IP[2]),  .DI(inport0[2]));
  C3I40 IN0_3 ( .PAD(inport0_IP[3]),  .DI(inport0[3]));

  C3I40 IN1_0 ( .PAD(inport1_IP[0]),  .DI(inport1[0]));
  C3I40 IN1_1 ( .PAD(inport1_IP[1]),  .DI(inport1[1]));
  C3I40 IN1_2 ( .PAD(inport1_IP[2]),  .DI(inport1[2]));
  C3I40 IN1_3 ( .PAD(inport1_IP[3]),  .DI(inport1[3]));

  C3I40 IN2_0 ( .PAD(inport2_IP[0]),  .DI(inport2[0]));
  C3I40 IN2_1 ( .PAD(inport2_IP[1]),  .DI(inport2[1]));
  C3I40 IN2_2 ( .PAD(inport2_IP[2]),  .DI(inport2[2]));
  C3I40 IN2_3 ( .PAD(inport2_IP[3]),  .DI(inport2[3]));

  C3I40 IN3_0 ( .PAD(inport3_IP[0]),  .DI(inport3[0]));
  C3I40 IN3_1 ( .PAD(inport3_IP[1]),  .DI(inport3[1]));
  C3I40 IN3_2 ( .PAD(inport3_IP[2]),  .DI(inport3[2]));
  C3I40 IN3_3 ( .PAD(inport3_IP[3]),  .DI(inport3[3]));

  C3I40 CON_0 ( .PAD(control_IP[0]),  .DI(control[0]));
  C3I40 CON_1 ( .PAD(control_IP[1]),  .DI(control[1]));

  C3O10 OUT_0 ( .DO(outport[0]),  .PAD(outport_OP[0])  );
  C3O10 OUT_1 ( .DO(outport[1]),  .PAD(outport_OP[1])  );
  C3O10 OUT_2 ( .DO(outport[2]),  .PAD(outport_OP[2])  );
  C3O10 OUT_3 ( .DO(outport[3]),  .PAD(outport_OP[3])  );

  HDNAN2D1 U19 ( .A1(n18), .A2(n19), .Z(outport[3]) );
```

- Adding new wire name in accordance with the IO ports name.
- Rename the IO ports, for example by adding at the end of the filename with “_IP” or “_OP” for input and output port respectively.
- Adding Power and Corner Pads.
- Instantiate new IO-pad cells.

Or Modify the file by adding IO Pad with Inline IO

```
module mux_4to1_4bit_PAD2 ( inport0_IP, inport1_IP, inport2_IP, inport3_IP, outport_OP, control_IP);
  input [3:0] inport0_IP;
  input [3:0] inport1_IP;
  input [3:0] inport2_IP;
  input [3:0] inport3_IP;
  output [3:0] outport_OP;
  input [1:0] control_IP;

  wire   n18, n19, n20, n21, n22, n23, n24, n25, n26, n27, n28, n29, n30, n31;
  wire [3:0] inport0, inport1, inport2, inport3, outport;
  wire [1:0] control;

  WCORNER SE_CORNER; WCORNER SW_CORNER; WCORNER NE_CORNER; WCORNER NW_CORNER;
  WVVDD VDD ();
  WVVSS VSS ();

  WC3I40 IN0_0 ( .PAD(inport0_IP[0]),  .DI(inport0[0]));
  WC3I40 IN0_1 ( .PAD(inport0_IP[1]),  .DI(inport0[1]));
  WC3I40 IN0_2 ( .PAD(inport0_IP[2]),  .DI(inport0[2]));
  WC3I40 IN0_3 ( .PAD(inport0_IP[3]),  .DI(inport0[3]));

  WC3I40 IN1_0 ( .PAD(inport1_IP[0]),  .DI(inport1[0]));
  WC3I40 IN1_1 ( .PAD(inport1_IP[1]),  .DI(inport1[1]));
  WC3I40 IN1_2 ( .PAD(inport1_IP[2]),  .DI(inport1[2]));
  WC3I40 IN1_3 ( .PAD(inport1_IP[3]),  .DI(inport1[3]));

  WC3I40 IN2_0 ( .PAD(inport2_IP[0]),  .DI(inport2[0]));
  WC3I40 IN2_1 ( .PAD(inport2_IP[1]),  .DI(inport2[1]));
  WC3I40 IN2_2 ( .PAD(inport2_IP[2]),  .DI(inport2[2]));
  WC3I40 IN2_3 ( .PAD(inport2_IP[3]),  .DI(inport2[3]));

  WC3I40 IN3_0 ( .PAD(inport3_IP[0]),  .DI(inport3[0]));
  WC3I40 IN3_1 ( .PAD(inport3_IP[1]),  .DI(inport3[1]));
  WC3I40 IN3_2 ( .PAD(inport3_IP[2]),  .DI(inport3[2]));
  WC3I40 IN3_3 ( .PAD(inport3_IP[3]),  .DI(inport3[3]));

  WC3I40 CON_0 ( .PAD(control_IP[0]),  .DI(control[0]));
  WC3I40 CON_1 ( .PAD(control_IP[1]),  .DI(control[1]));

  WC3010 OUT_0 ( .DO(outport[0]),  .PAD(outport_OP[0])  );
  WC3010 OUT_1 ( .DO(outport[1]),  .PAD(outport_OP[1])  );
  WC3010 OUT_2 ( .DO(outport[2]),  .PAD(outport_OP[2])  );
  WC3010 OUT_3 ( .DO(outport[3]),  .PAD(outport_OP[3])  );

  HDNAN2D1 U19 ( .A1(n18), .A2(n19), .Z(outport[3]) );
```

- Adding new wire name in accordance with the IO ports name.
- Rename the IO ports, for example by adding at the end of the filename with “_IP” or “_OP” for input and output port respectively.
- Adding Power and Corner Pads.
- Instantiate new IO-pad cells.

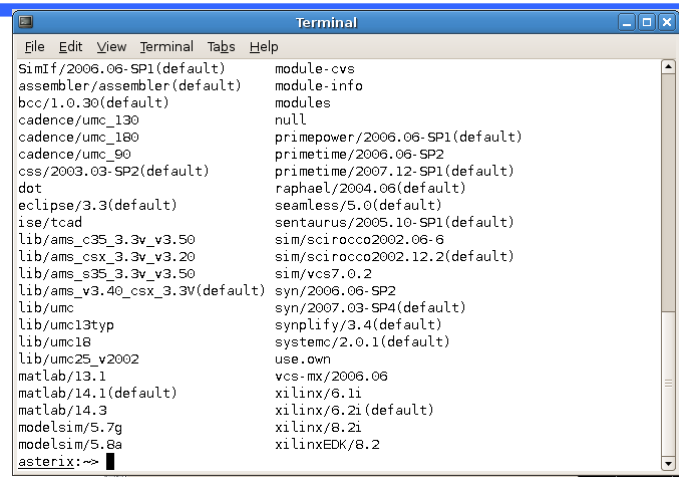
File Preparation: create IO Assignment file

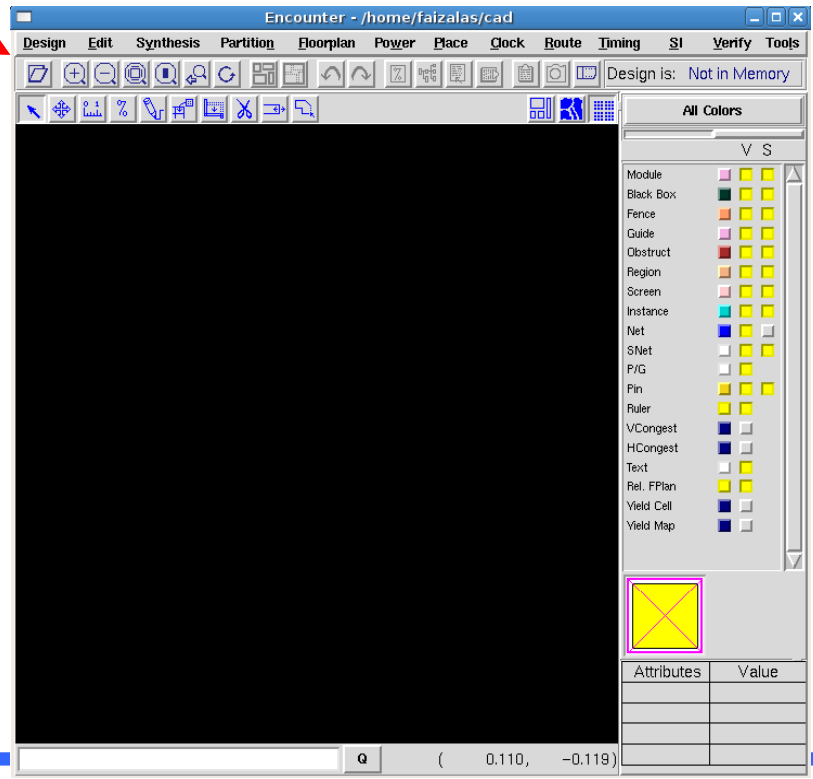
File name e.g., mux_4to1_4bit.io

```
Version: 2

Pad: NE_CORNER  NE
Pad: NW_CORNER  NW
Pad: SE_CORNER  SE
Pad: SW_CORNER  SW

Pad: VDD        N
Pad: VSS        N
Pad: OUT_0      N
Pad: OUT_1      N
Pad: OUT_2      N
Pad: OUT_3      N

Pad: IN0_0      S
Pad: IN0_1      S
Pad: IN0_2      S
Pad: IN0_3      S
Pad: IN1_0      S
Pad: IN1_1      S

Pad: IN1_2      W
Pad: IN1_3      W
Pad: IN2_0      W
Pad: IN2_1      W
Pad: IN2_2      W
Pad: IN2_3      W

Pad: IN3_0      E
Pad: IN3_1      E
Pad: IN3_2      E
Pad: IN3_3      E
Pad: CON_0      E
Pad: CON_1      E
```

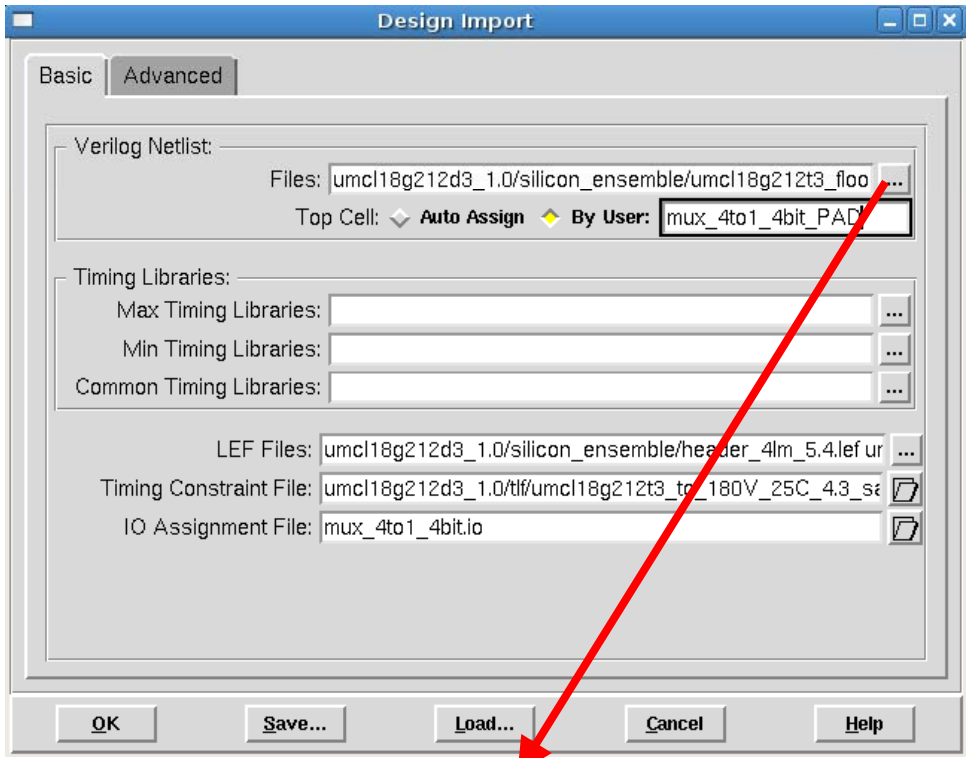
Starting Cadence Silicon Encounter

- Create a working directory
  - `mkdir cad`
  - `cd cad`
- Start the environment
  - `module load cadence/umc_180`
  - `encounter`

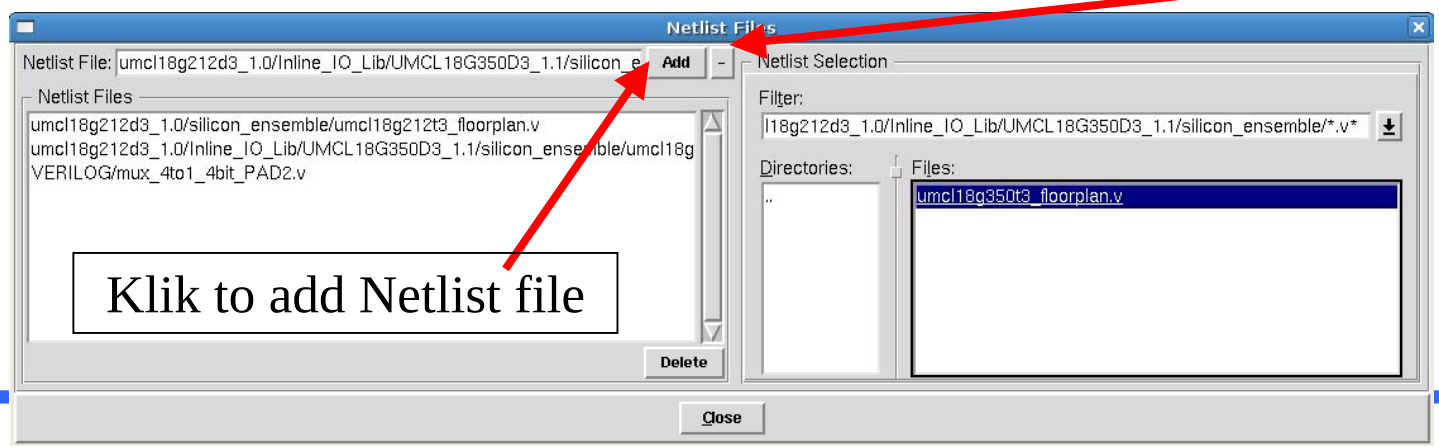




Design Import: Verilog Netlist File



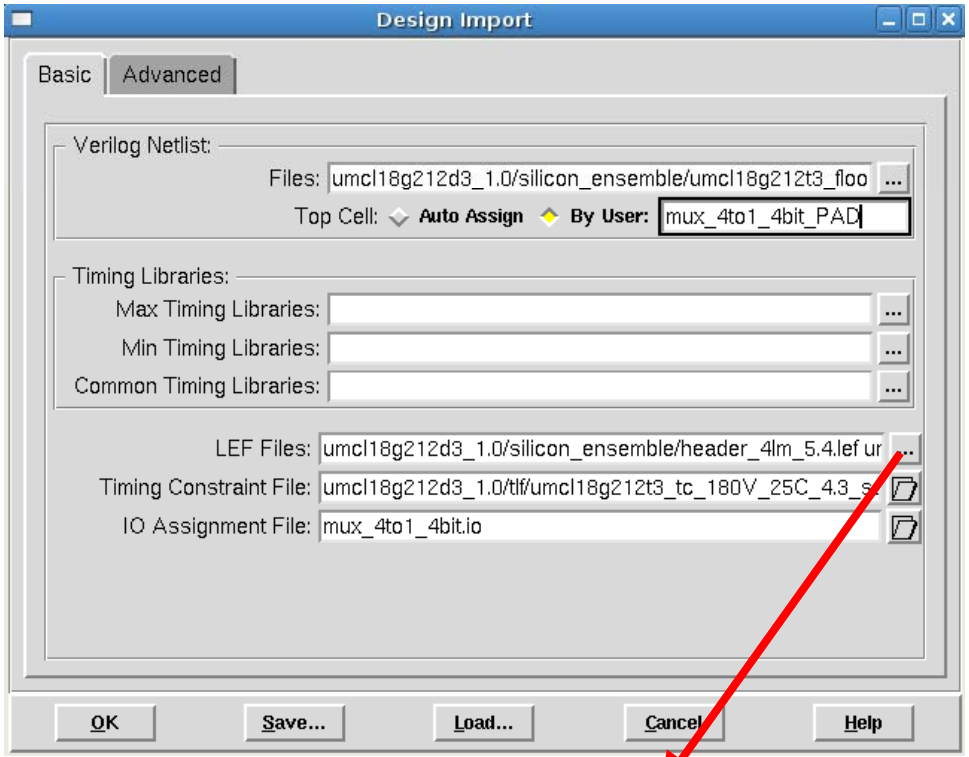
- Klik Design > Design Import ...
- Verilog Netlist files that must be import are:
  - `Standard-cell floorplan file: “umcl18g212t3_floorplan.v”`
  - `IO-Pad cell floorplan file: “umc118g350t3_floorplan.v” (INLINE IO PAD)`
  - `Your structural file with IO pad: “mux_4to1_4bit_PAD.v”`

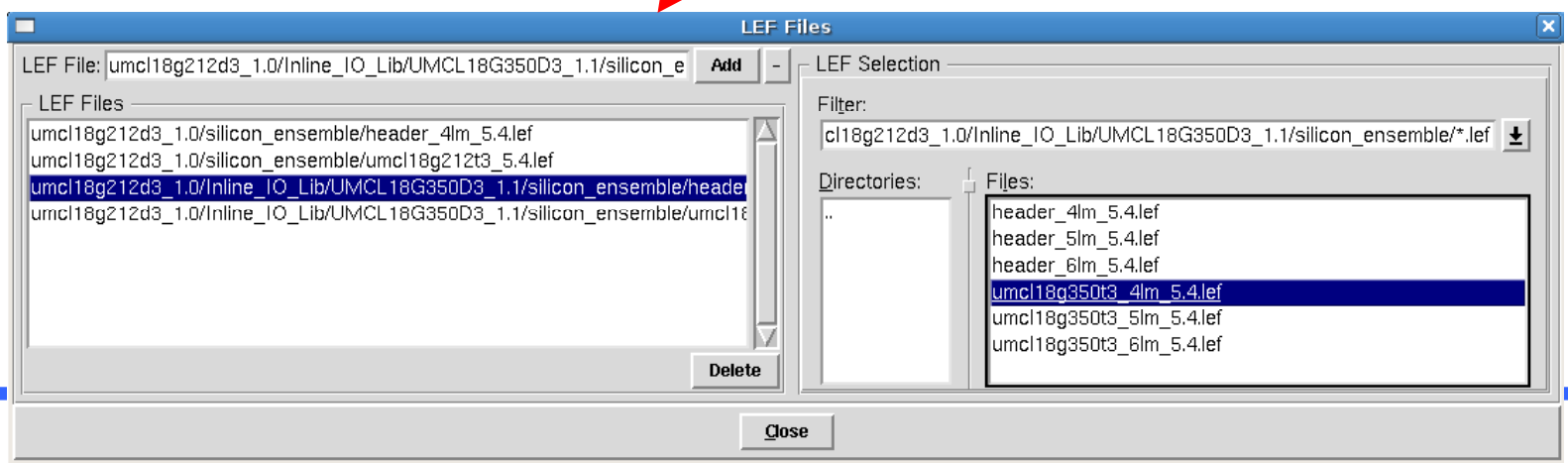


Klik to add Netlist file

Klik to view Netlist Selection

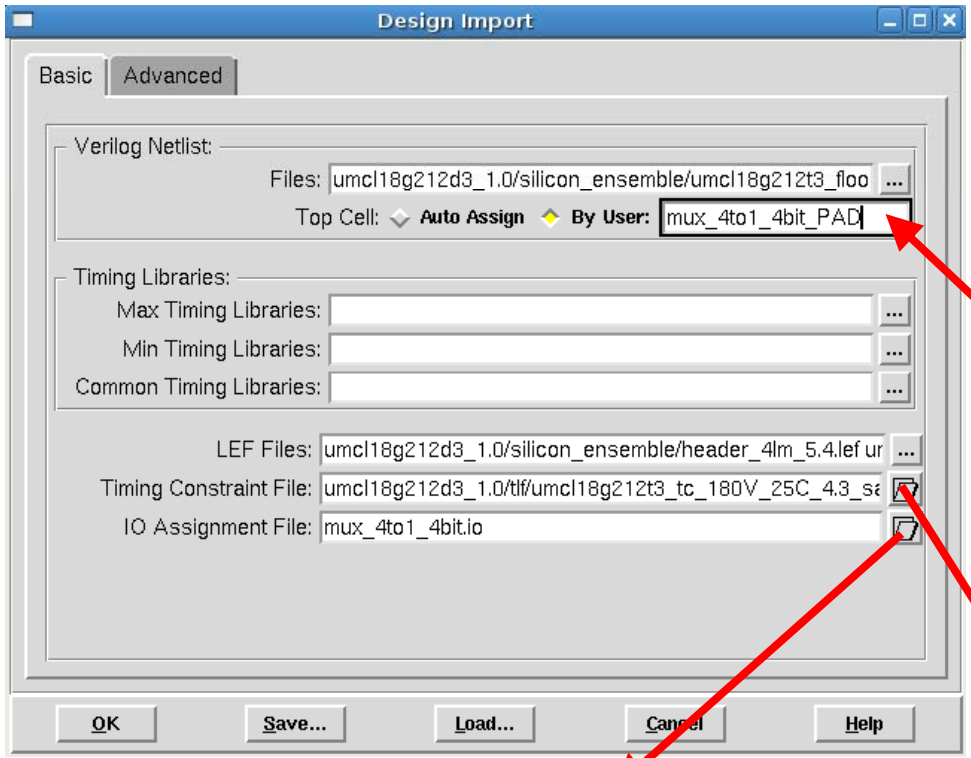
Design Import: LEF Files

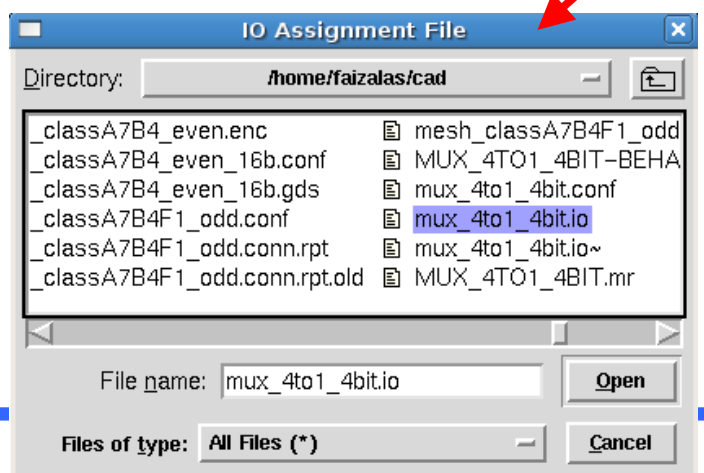


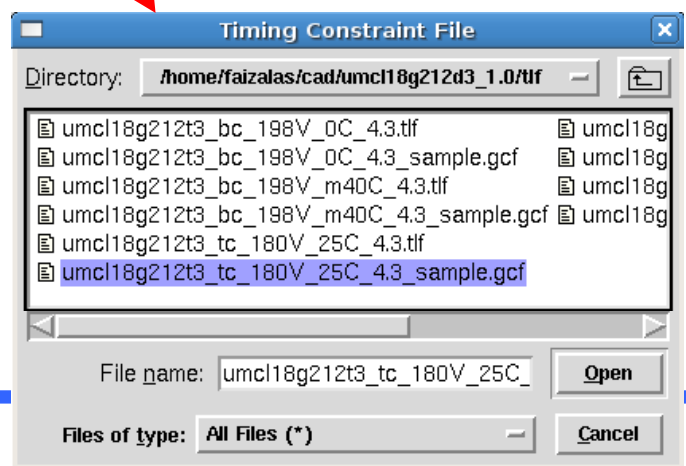


- LEF Files that must be used are LEF files for standard-cell and IO-pad cells:
- Standard-cell LEF files:
  - "`header_4lm_5.4.lef`"
  - "`umcl18g212t3_5.4.lef`"
- IO-Pad cell LEF files:
  - "`header_4lm_5.4.lef`"
  - "`umcl18g350t3_4lm_5.4.lef`" (**`INLINE IO PAD`**)

Design Import: Timing Constaint & IO Assignment File

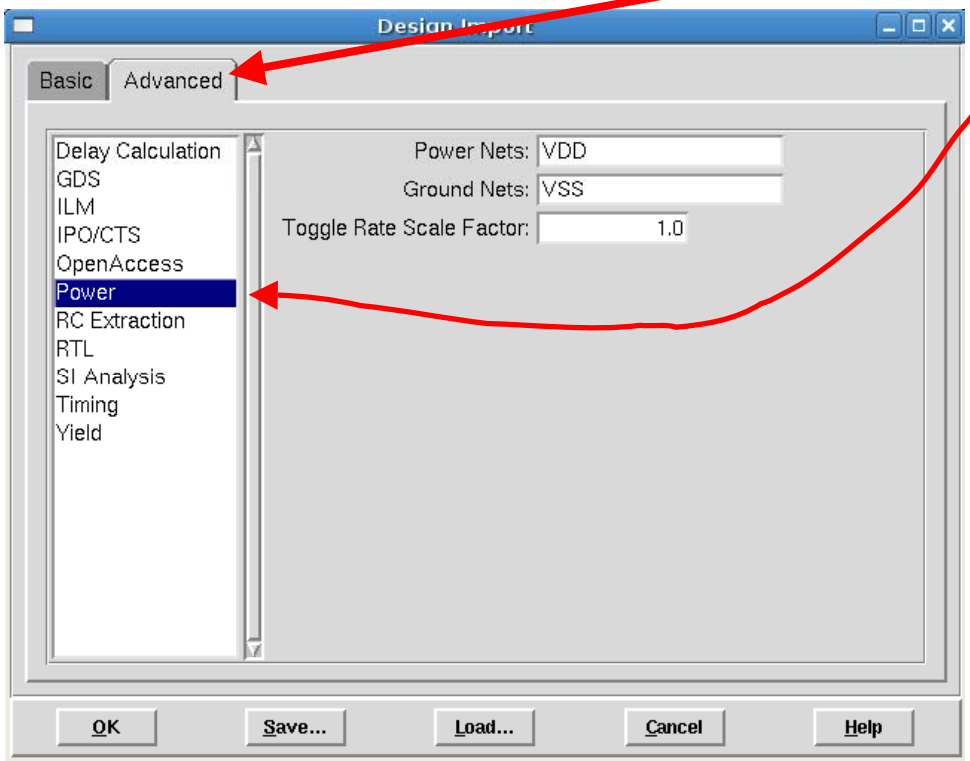






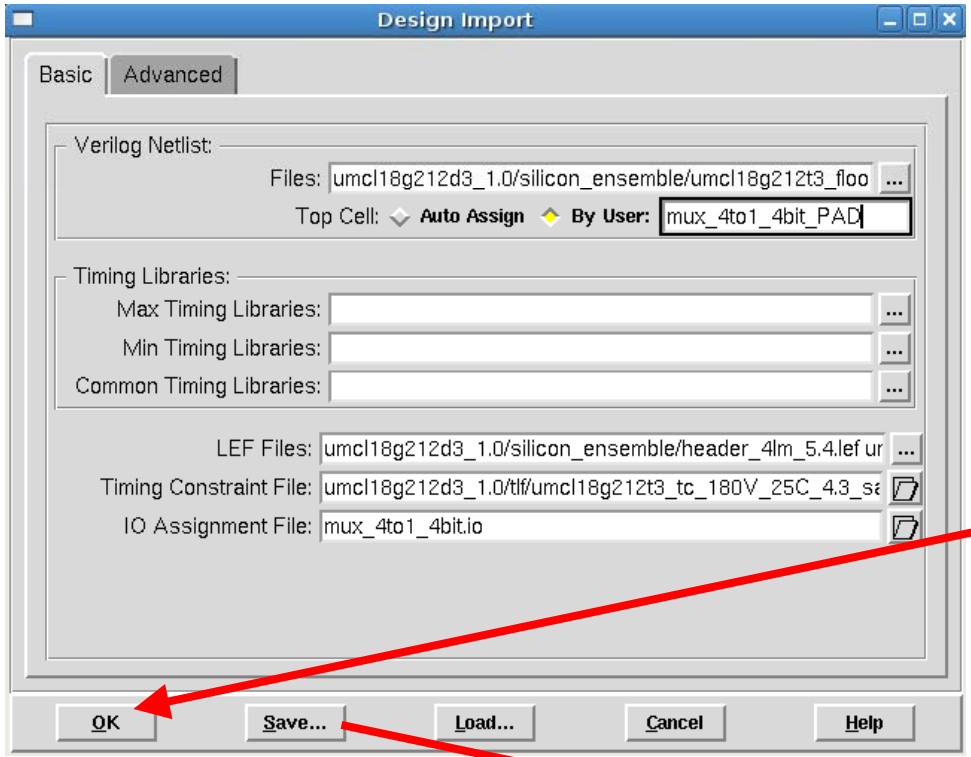
- Timing Constraint File
  - `mkdir cad`
  - `cd cad`
- IO Assignment File
  - `module load cadence/umc_180`
  - `Encounter`
- Give the top cell name (in general, the name must be the same as the top module name).

Power & Ground Name

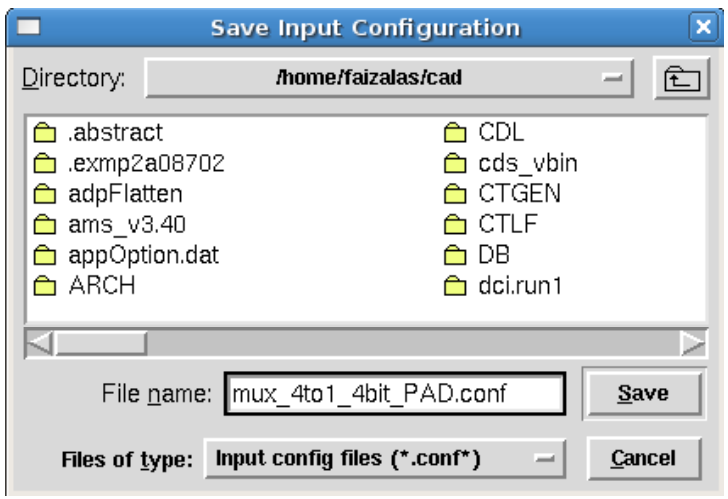


- Klik: Advanced Button
- Klik Power Menu
- Give the name for Power Nets and Ground Nets. For Instance, VDD and VSS

Save Design Import Configuration

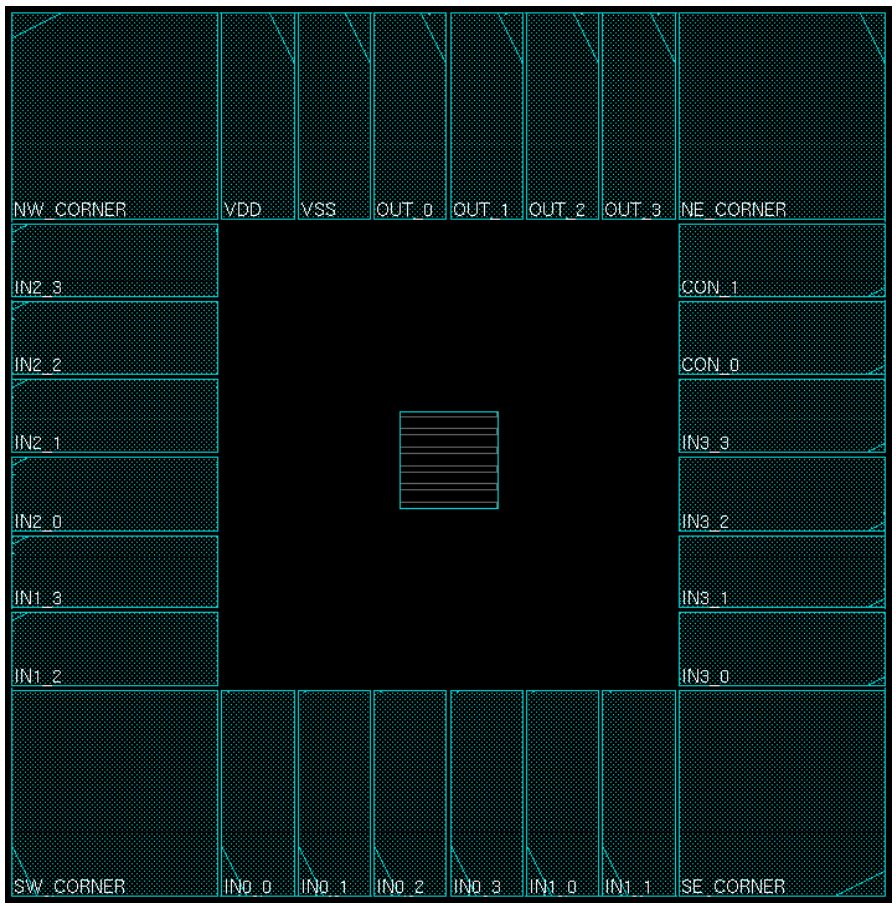


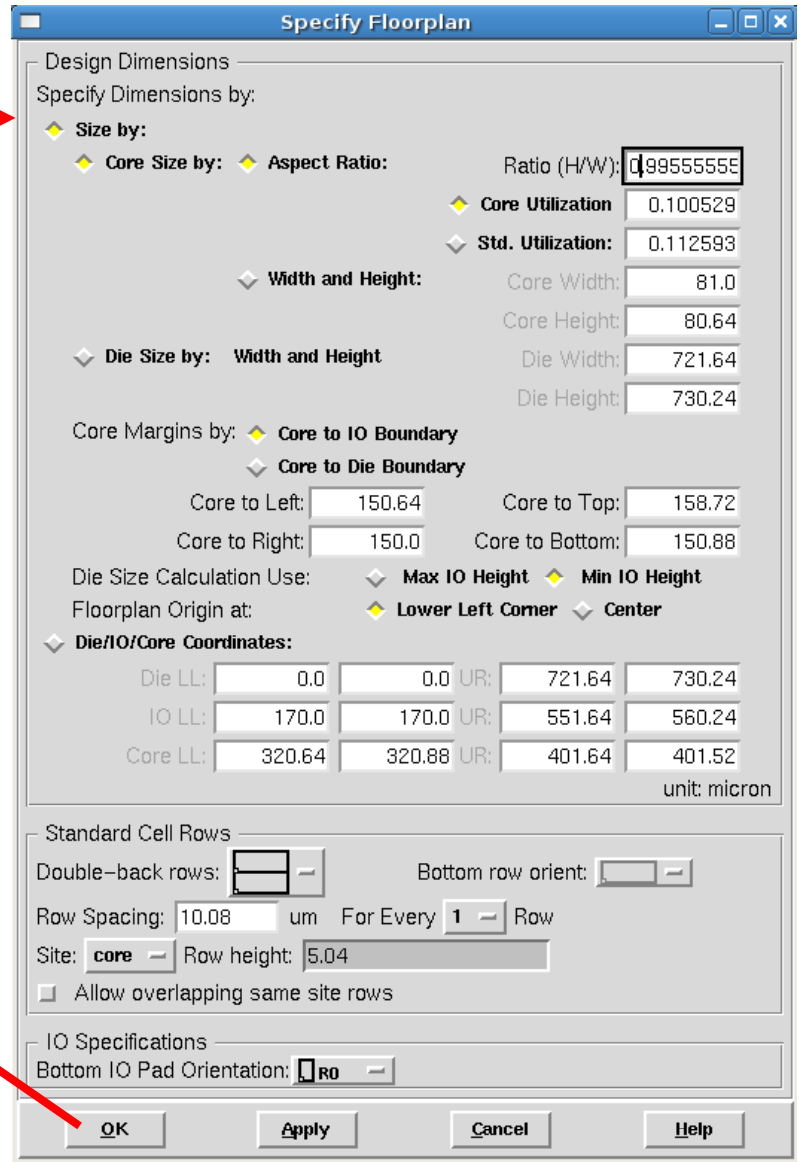
- Klik: Save... to save your design import configuration.
  - `Save input configuration window appears.`
  - `Give file name with *.conf extension, for example: “mux_4to1_4bit_PAD.conf”`
- Klik: OK to import the design.



Specifiy Floorplanning

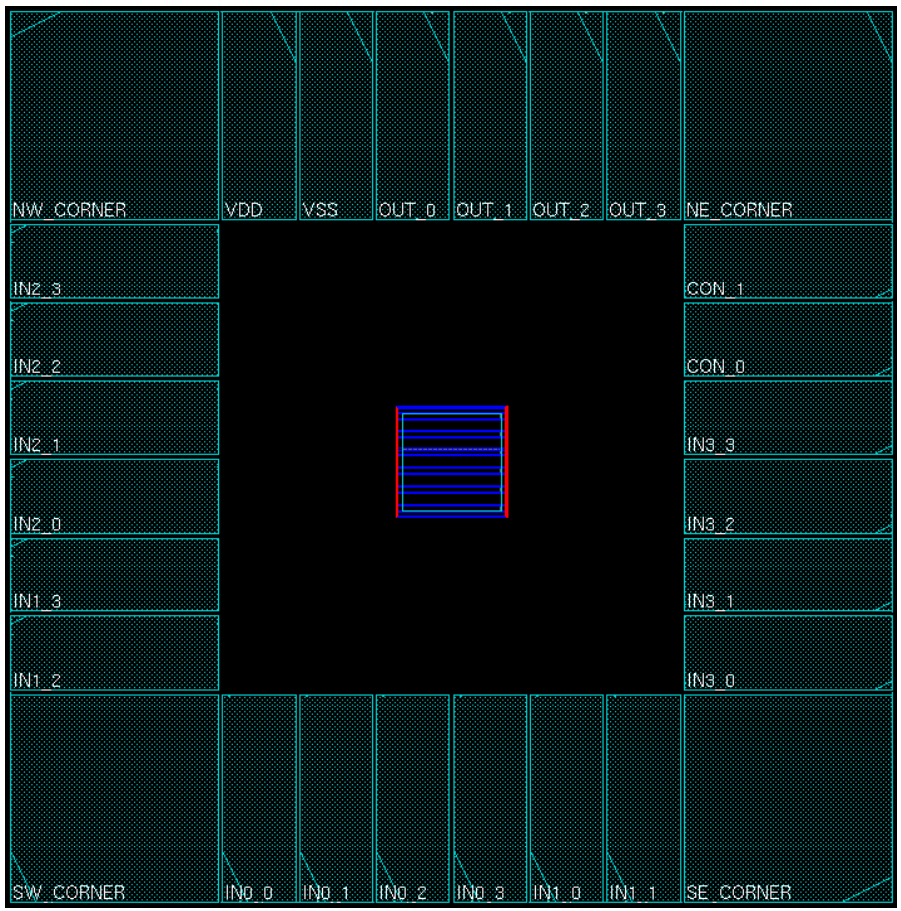
- Klik: Floorplan > Specify Floorplan, the Specifiy floorplan window appears.

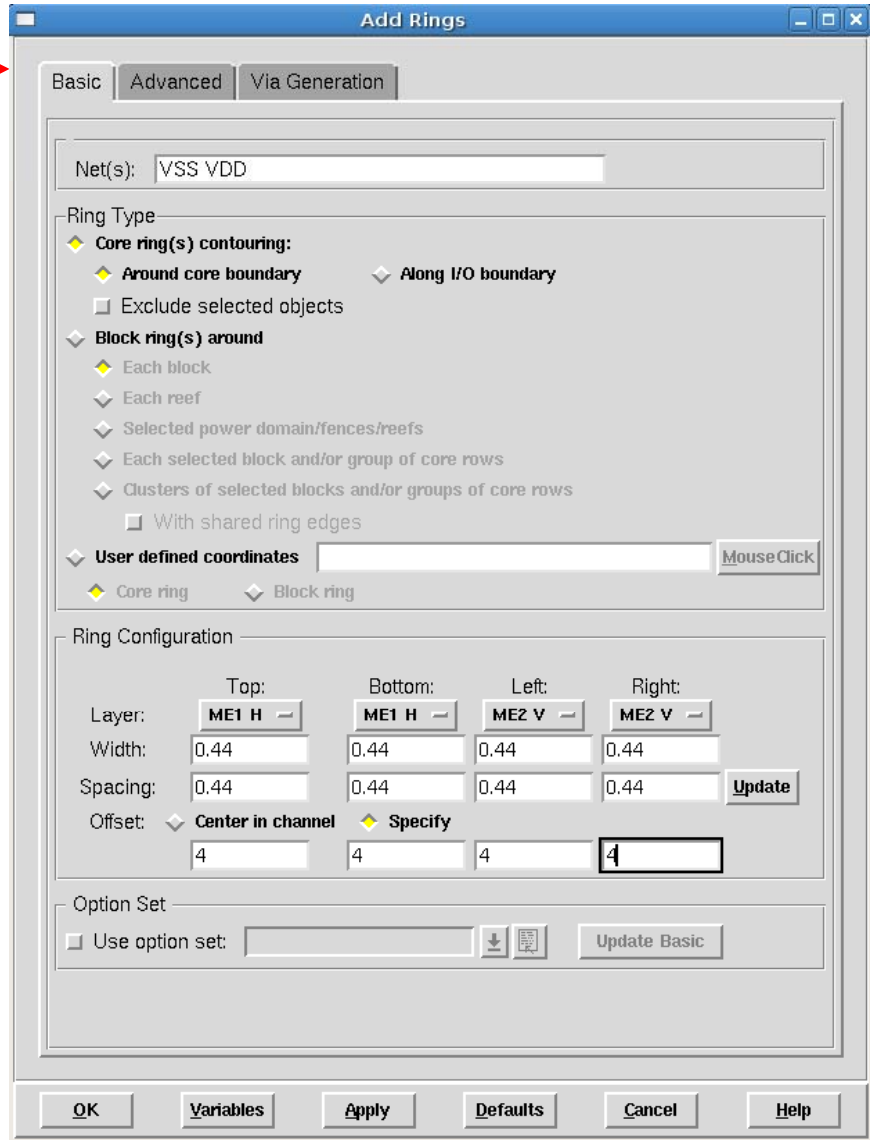




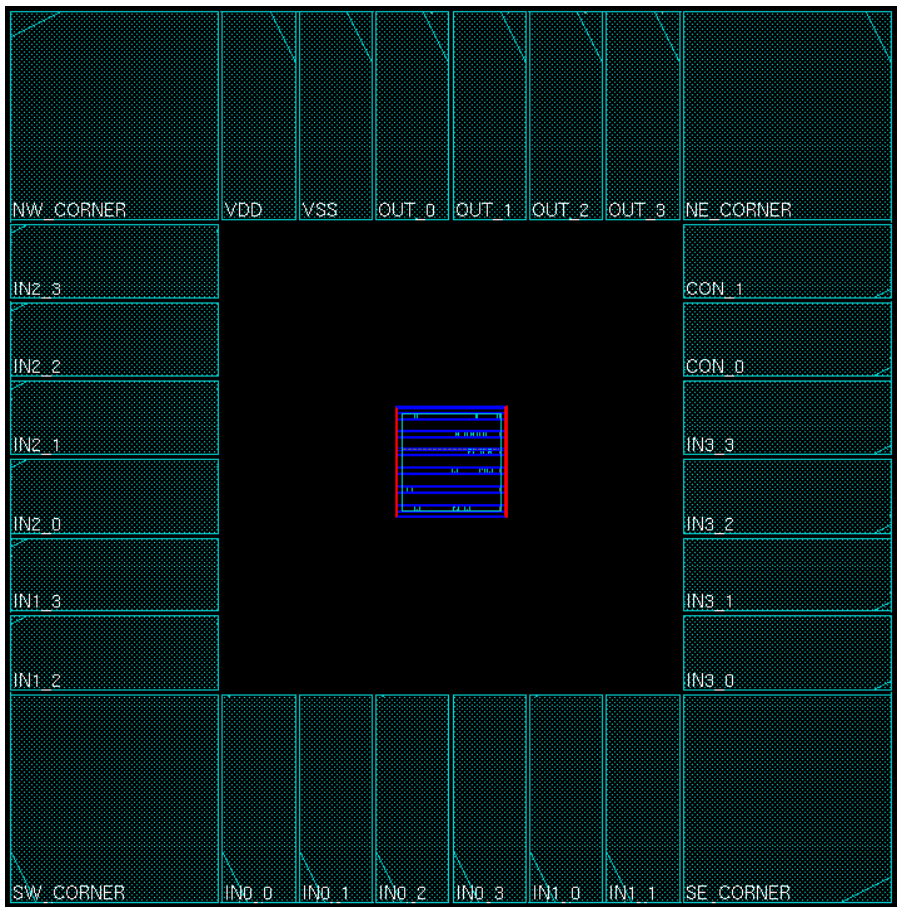
Power Ring Creation and Route

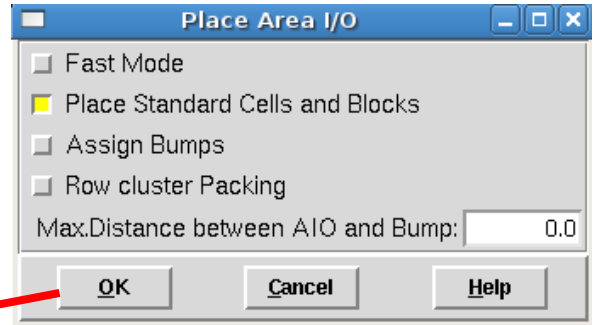
- Klik: Power > Power Planning > Add Rings, then the window appears.
- Klik: Route > Special Route ..., then the Sroute window appears. Klik OK.





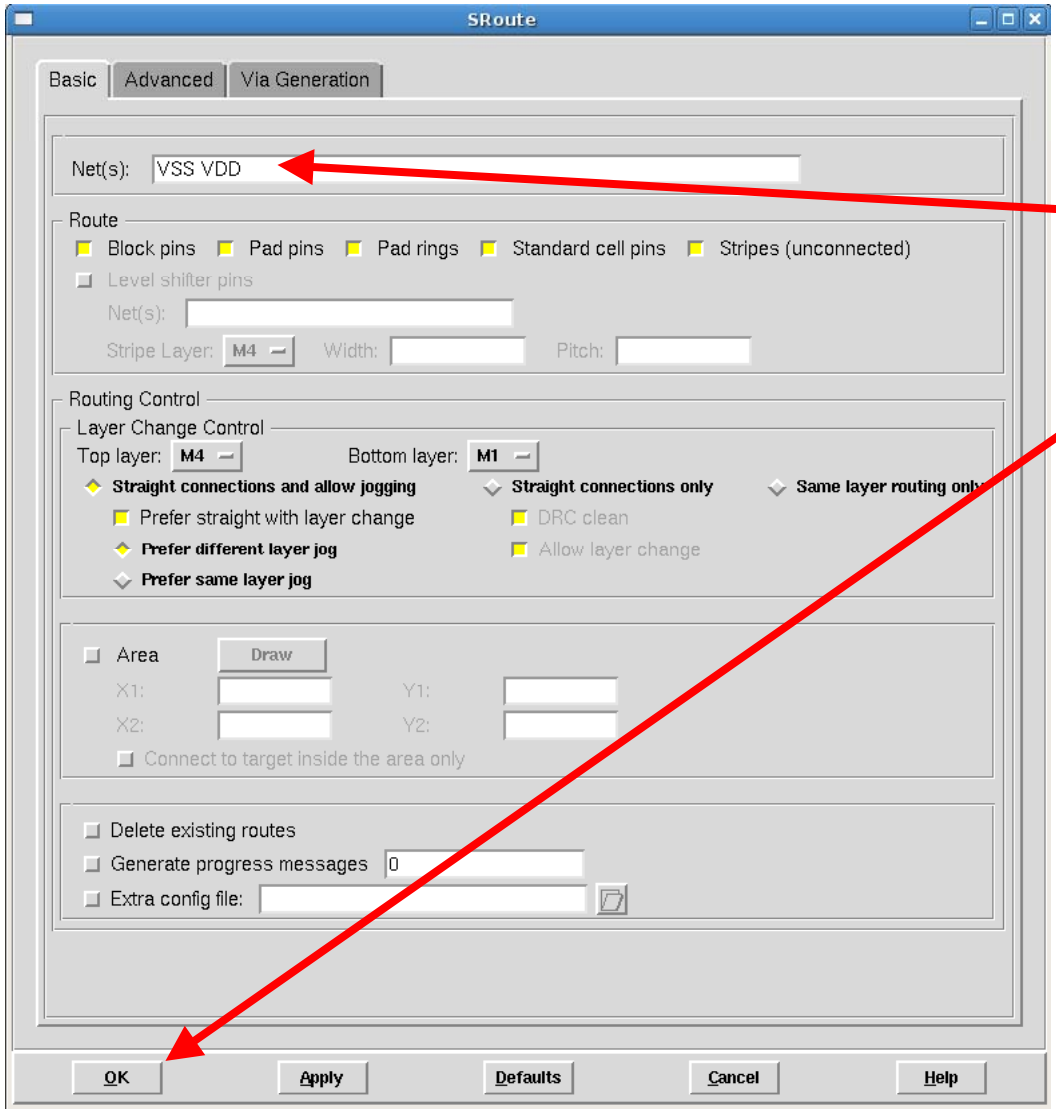
Place Standard-Cell Blocks and Area I/O





- Klik: Place > Area I/O...
- Then klik: Place > Display > Display Spare Cells to see the cell placement result

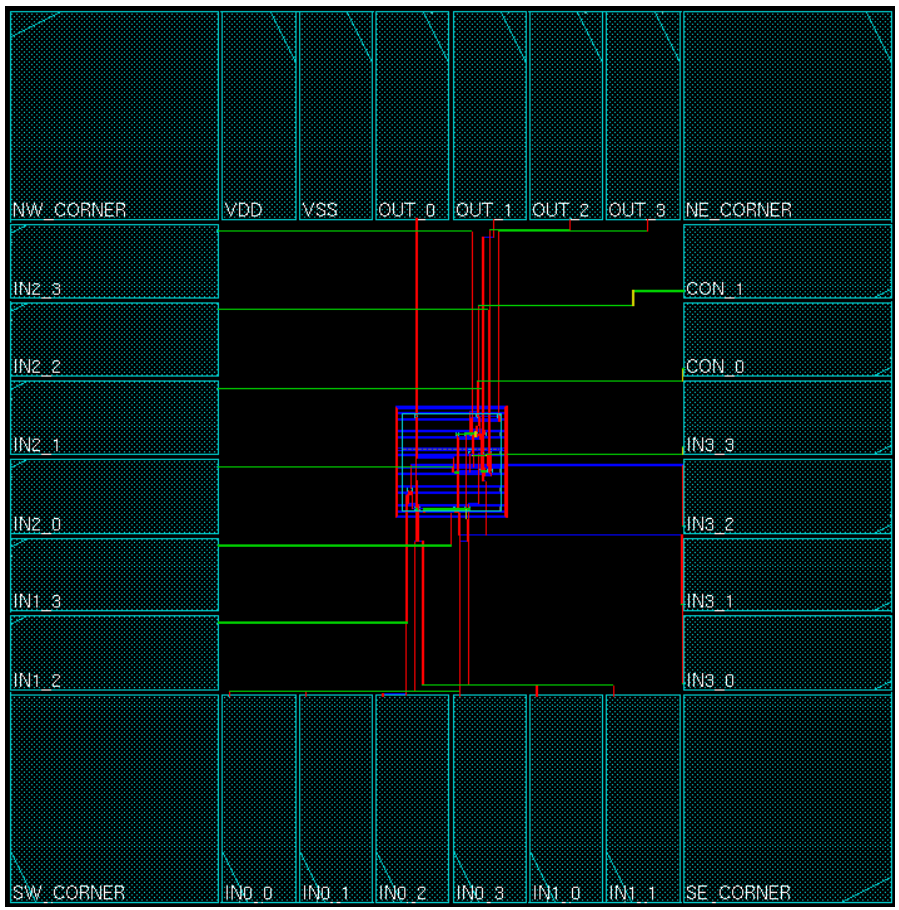
Special Route: Power Route Again

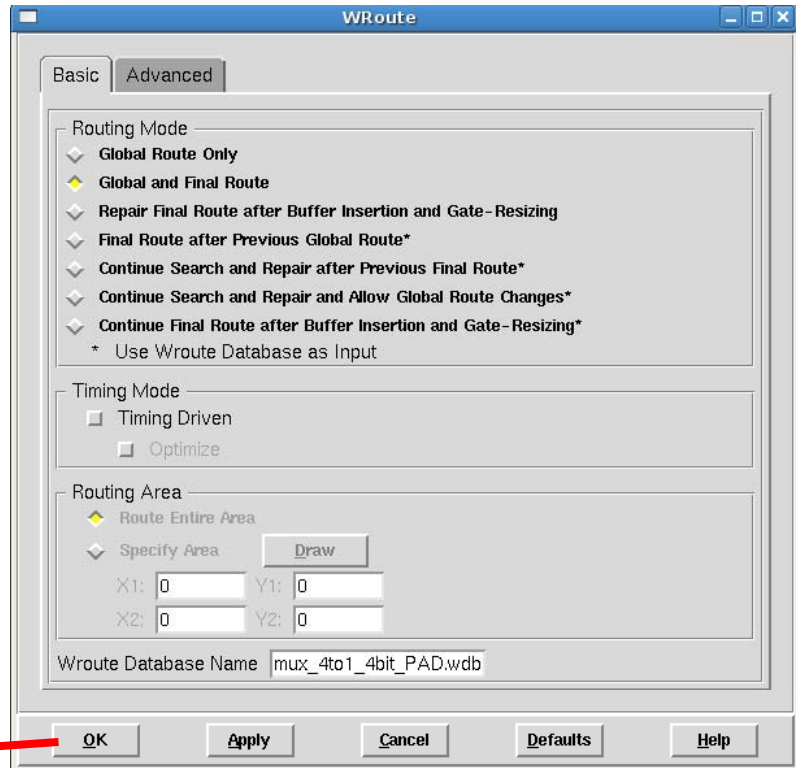


- Klik: Route > Special Route …, then the Sroute window appears.
- Check that the Power and Ground Nets names are appears in the window.
- Klik: OK

Global and Final Route

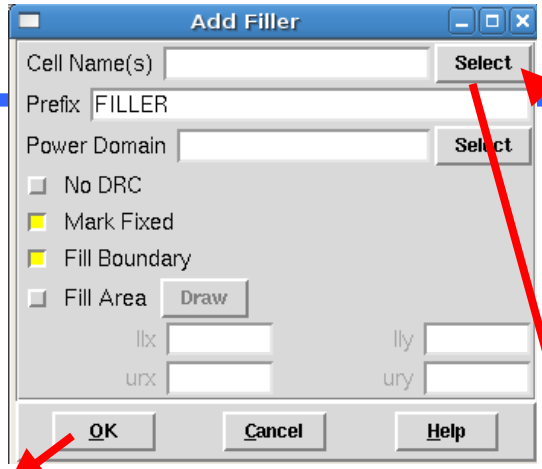
- Klik: Route > WRoute

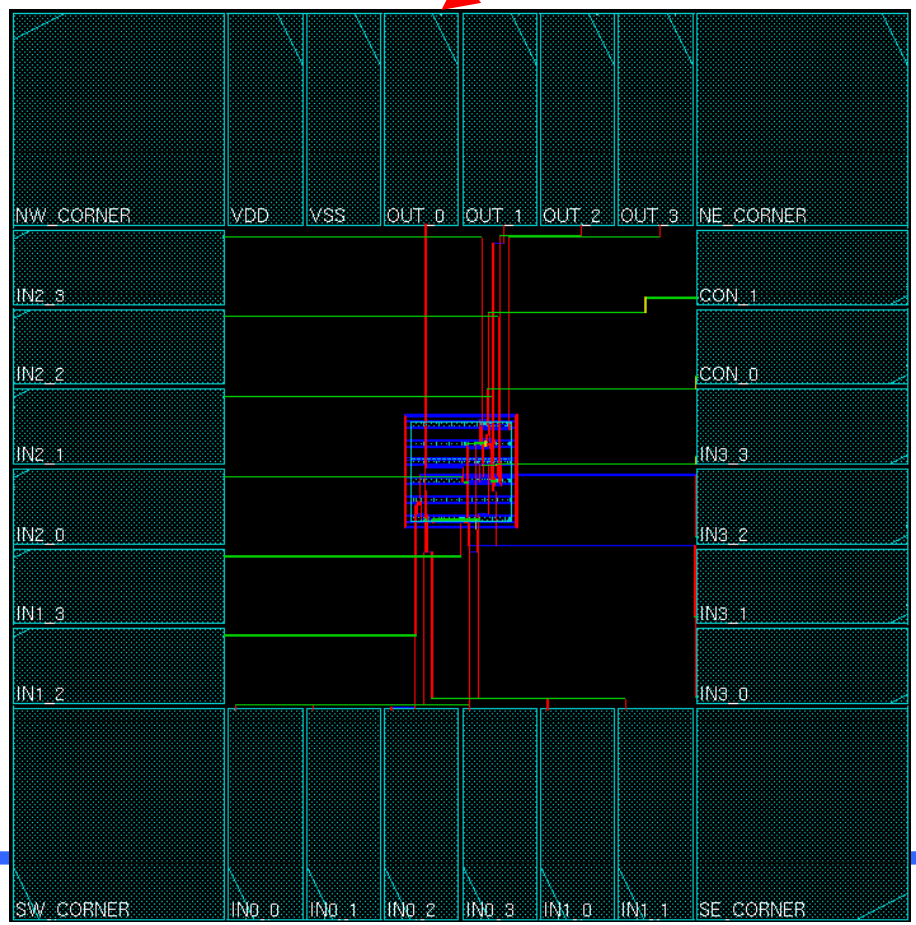


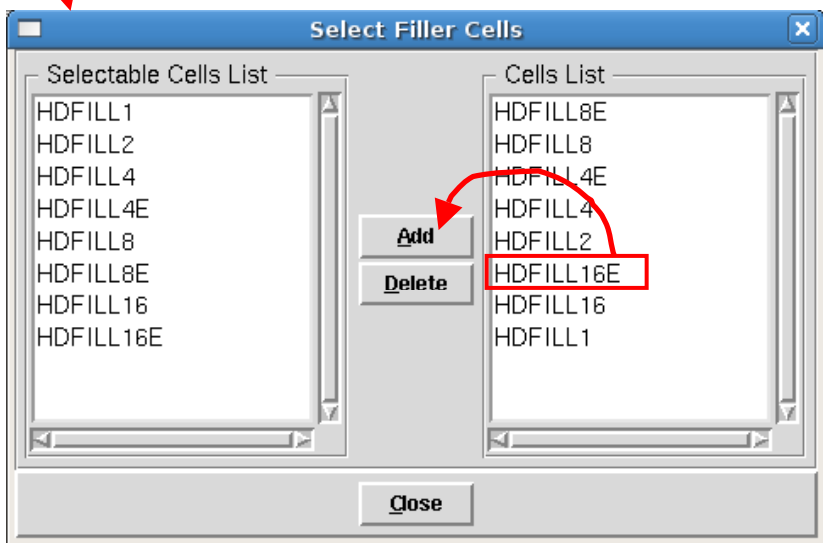


Adding Filler Cells

- Klik: Place > Filler > Add .. Menu, then Add Filler window appears.
- Klik Select, then Select Filler Cells window appears.
- Add All Cells list by select the HDFILL cell then click Add button. Then Close the windows.
- Klik OK.







Verify the Design

- Klik Verify > Verifiy Connectivity, then Klik OK.
- Klik Verify > Verifiy Metal Density, then Klik OK.
- Klik Verify > Verifiy Geometry, then Klik OK.

Terminal

File Edit View Terminal Tabs Help

```
encounter 1>
******** Start: VERIFY CONNECTIVITY ********
Start Time: Mon Feb 25 18:50:05 2008

Design Name: mux_4to1_4bit_PAD2
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (721.6400, 730.2400)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Mon Feb 25 18:50:05 2008
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)

encounter 1>
```

Terminal

File Edit View Terminal Tabs Help

```
******** End: VERIFY DENSITY ********
 (CPU Time: 0:00:00.0  MEM: 0.000M)

encounter 1> setMetalFill -layer 1 -windowSize 1000.000 1000.000 -windowStep 50.000 50.000 -min
Density 25.000 -maxDensity 80.000
setMetalFill -layer 2 -windowSize 1000.000 1000.000 -windowStep 50.000 50.000 -minDensity 25.00
0 -maxDensity 80.000
setMetalFill -layer 3 -windowSize 1000.000 1000.000 -windowStep 50.000 50.000 -minDensity 25.00
0 -maxDensity 80.000
setMetalFill -layer 4 -windowSize 1000.000 1000.000 -windowStep 50.000 50.000 -minDensity 25.00
0 -maxDensity 80.000

******** Start: VERIFY DENSITY ********
verify density in ... window 1 out of 1
No density violations were found.

******** End: VERIFY DENSITY ********
 (CPU Time: 0:00:00.0  MEM: 0.000M)

encounter 1>
```

Terminal

File Edit View Terminal Tabs Help

```
encounter 1>  *** Starting Verify Geometry (MEM: 100.8) ***

  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 4160
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.


********************************************************************************
WARNING:

Pin of Cell "FILLER_26" at (320.850, 350.520), (321.160, 351.720) on Layer "M1" is not connected to any net
.

Please use connectToGlobalNet or GUI FloorPlan->Global Net Connections to specify global net connection rul
es properly.

********************************************************************************


  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.1  MEM: 0.0M)

encounter 1>
```

Save the layout result to GDS file

- Klik: Design > Save > GDS.., then GDS Export window appears.
- Klik the button, then Stream File window appears.
- Select the directory, where you want to save the file.
- Give the file name (*.gds), for example: mux_4to1_4bit.gds
- This file can be exported into Cadence Virtuoso for further editing.