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| --- |
| **RESET:** |
| RegReset  = 1 |
| A\_reset = 1 |
| B\_reset = 1 |
| PC\_reset = 1 |
| E\_PC\_reset = 1 |
| MDR\_reset = 1 |
| ALUOut\_reset = 1 |
| MulReg\_reset = 1 |
| IR\_reset = 1 |

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| **STACK\_INIT:** |
| RegWrite = 1 |
| MemtoReg = 001 |
| RegDst = 10 |

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| **FETCH:** |
| IorD = 00 |
| wr = 0 |

**FETCH\_MEM\_DELAY1:** 0

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| **FETCH\_MEM\_DELAY2:** |
| PCWrite = 1 |
| IRWrite = 1 |
| ALU\_sel = 001 |
| PCSource = 000 |
| ALUSrcA = 0 |
| ALUSrcB = 01 |
| MDR\_load = 1 |

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| **DECODE:** |
| ALU\_sel = 001 |
| ALUSrcA = 0 |
| ALUSrcB = 11 |
| ALUOutSrc = 00 |
| A\_load = 1 |
| B\_load = 1 |
| ALUOut\_load = 1 |

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| --- |
| **TREATING\_OVERFLOW\_1:** |
| ALU\_sel = 010 |
| ALUSrcA = 0 |
| ALUSrcB = 01 |
| E\_PC\_load = 1 |

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| **TREATING\_OVERFLOW\_2:** |
| wr = 0 |
| IorD = 10 |

**OVERFLOW\_EXCEPTION\_DELAY1:** 0

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| **OVERFLOW\_EXCEPTION\_DELAY2:** |
| MDR\_load = 1 |

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| --- |
| **LOAD\_PC\_OVERFLOW\_EXCEPTION:** |
| PCWrite = 1 |
| PCSource = 101 |

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| --- |
| **TREATING\_INVALID\_OP\_1:** |
| ALU\_sel = 010 |
| ALUSrcA = 0 |
| ALUSrcB = 01 |
| E\_PC\_load = 1 |

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| **TREATING\_INVALID\_OP\_2:** |
| wr = 0 |
| IorD = 10 |

**OP\_EXCEPTION\_DELAY1:** 0

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| **OP\_EXCEPTION\_DELAY2:** |
| MDR\_load = 1 |

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| **LOAD\_PC\_OP\_EXCEPTION:** |
| PCWrite = 1 |
| PCSource = 101 |

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| --- |
| **ADD:** |
| ALU\_sel  = 001 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOutSrc = 00 |
| ALUOut\_load = 1 |

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| **R\_WAIT:** |
| RegWrite = 1 |
| MemtoReg = 000 |
| RegDst = 01 |

**NOP:** 0

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| --- |
| **AND:** |
| ALU\_sel = 011 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOutSrc = 00 |
| ALUOut\_load = 1 |

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| --- |
| **SUB:** |
| ALU\_sel = 010 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOutSrc = 00 |
| ALUOut\_load = 1 |

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| --- |
| **XOR:** |
| ALU\_sel = 110 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOutSrc = 00 |
| ALUOut\_load = 1 |

**BREAK:** 0

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| --- |
| **J:** |
| PCWrite = 1 |
| ALU\_sel = 001 |
| PCSource = 010 |
| ALUSrcA = 0 |
| ALUSrcB = 11 |
| IorD = 01 |
| ALUOutSrc = 00 |
| IorD = 1 |

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| --- |
| **JAL\_COMP:** |
| ALU\_sel = 000 |
| ALUSrcA = 0 |
| ALUSrcB = 01 |
| IorD = 00 |
| RegDst = 11 |
| ALUOut\_load = 1 |

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| --- |
| **JAL\_WR31:** |
| PCWrite = 1 |
| REgWrite = 1 |
| PCSource = 010 |
| ALU\_sel = 000 |
| ALUSrcA = 0 |
| RegDst = 11 |

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| --- |
| **JR:** |
| PCWrite = 1 |
| wr = 0 |
| IRWrite = 0 |
| ALU\_sel = 001 |
| PCSource = 100 |
| ALUSrcA = 1 |
| ALUSrcB = 01 |
| ALUOutSrc = 00 |
| IorD = 01 |
| ALUOut\_load = 1 |

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| --- |
| **BEQ:** |
| PCWriteCond = 1 |
| ALU\_sel = 010 |
| PCSource = 001 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOutSrc = 00 |
| ALUOut\_load = 0 |

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| --- |
| **BNE:** |
| PCWriteCond = 1 |
| ALU\_sel = 010 |
| PCSource = 01 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOutSrc = 00 |
| ALUOut\_load = 0 |

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| --- |
| **LUI:** |
| RegWrite = 1 |
| MemtoReg = 010 |
| RegDst = 00 |

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| --- |
| **SW\_ADDRESS\_COMP:** |
| ALU\_sel = 001 |
| ALUSrcA = 1 |
| ALUSrcB = 10 |
| ALUOutSrc = 00 |
| ALUOut\_load = 1 |

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| --- |
| **SW:** |
| wr = 1 |
| IorD = 01 |

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| --- |
| **LW\_ADDRESS\_COMP:** |
| ALU\_sel = 001 |
| ALUSrcA = 1 |
| ALUSrcB = 10 |
| ALUOutSrc = 00 |
| ALUOut\_load = 1 |

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| --- |
| **LW:** |
| wr = 0 |
| IorD = 01 |

**LW\_DELAY1:** 0

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| --- |
| **LW\_DELAY2:** |
| MDR\_load = 1 |

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| --- |
| **WRITE\_BACK:** |
| RegWrite = 1 |
| MemtoReg = 001 |
| RegDst = 00 |

**DEFAULT:** 0

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| --- |
| **MULT0:** |
| workMUult = 1 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| MulReg\_load = 1 |

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| --- |
| **MULT1:** |
| ALUSrcA = 1 |
| ALUSrcB = 0 |
| workMult = 2 |
| MulReg\_load = 1 |

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| --- |
| **MFHI:** |
| workMult = 1 |
| ALU\_sel = 000 |
| ALUSrcA = 0 |
| ALUSrcB = 00 |
| ALUOutSrc = 10 |
| ALUOut\_load = 1 |

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| --- |
| **MHLO:** |
| workMult = 1 |
| ALUOutSrc = 11 |
| ALUOut\_load = 1 |

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| --- |
| **MFSTORE:** |
| RegWrite = 1 |
| workMult = 1 |
| RegDst = 01 |

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| --- |
| **RTE:** |
| PCWrite = 1 |
| PCSource = 011 |

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| --- |
| **SB\_ADDRESS\_COMP:** |
| ALU\_sel = 3'b001 |
| ALUSrcA = 1'b1 |
| ALUSrcB = 2'b10 |
| ALUOutSrc = 2'b00 |
| ALUOut\_load = 1 |

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| --- |
| **SB\_DELAY1:** |
| wr = 0 |
| IorD = 01 |

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| --- |
| **SB\_DELAY2:** |
| wr = 0 |
| IorD = 01 |

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| --- |
| **SB\_DELAY3:** |
| wr = 0 |
| IorD = 01 |
| MDR = 1 |

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| --- |
| **SB\_WRITE:** |
| IorD = 01 |
| wr = 1 |
| MemDataSize = 01 |

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| --- |
| **SH\_ADDRESS\_COMP:** |
| ALU\_sel = 001 |
| ALUSrcA = 1 |
| ALUSrcB = 10 |
| ALUOutSrc = 00 |
| ALUOut\_load = 1 |

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| --- |
| **SH\_DELAY1:** |
| wr = 0 |
| IorD = 01 |

|  |
| --- |
| **SH\_DELAY2:** |
| wr = 0 |
| IorD = 2'b01 |

|  |
| --- |
| **SH\_DELAY3:** |
| wr = 0 |
| IorD = 01 |
| MDR = 1 |

|  |
| --- |
| **SH\_WRITE:** |
| IorD = 01 |
| wr = 1 |
| MemDataSize = 10 |