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| --- |
| **RESET:** |
| RegReset = 1 |
| A\_reset = 1 |
| B\_reset = 1 |
| PC\_reset = 1 |
| MDR\_reset = 1 |
| ALUOut\_reset = 1 |
| IR\_reset = 1 |

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| **ADD:** |
| ALU\_sel = 001 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOut\_load = 1 |

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| **R\_WAIT:** |
| RegWrite = 1 |
| MemtoReg = 00 |
| RegDst = 1 |

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| --- |
| **NOP:** |
| PCWriteCond = 0 |
| PCWrite = 0 |
| wr = 0 |
| IRWrite = 0 |
| RegWrite = 0 |
| RegReset = 0 |
| A\_load = 0 |
| A\_reset = 0 |
| B\_load = 0 |
| B\_reset = 0 |
| PC\_reset = 0 |
| MDR\_load = 0 |
| MDR\_reset = 0 |
| ALUOut\_load = 0 |
| ALUOut\_reset = 0 |
| IR\_reset = 0 |

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| **AND:** |
| ALU\_sel = 011 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOut\_load = 1 |

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| **SUB:** |
| ALU\_sel = 010 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOut\_load = 1 |

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| **XOR:** |
| ALU\_sel = 110 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOut\_load = 1 |

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| **BREAK:** |
| PCWriteCond = 0 |
| PCWrite = 0 |
| wr = 0 |
| IRWrite = 0 |
| RegWrite = 0 |
| RegReset = 0 |
| A\_load = 0 |
| A\_reset = 0 |
| B\_load = 0 |
| B\_reset = 0 |
| PC\_reset = 0 |
| MDR\_load = 0 |
| MDR\_reset = 0 |
| ALUOut\_load = 0 |
| ALUOut\_reset = 0 |
| IR\_reset = 0 |

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| --- |
| **J:** |
| PCWrite = 1 |
| ALU\_sel = 001 |
| PCSource = 10 |
| ALUSrcA = 0 |
| ALUSrcB = 11 |
| IorD = 1 |
| ALUOut\_load = 1 |

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| --- |
| **BEQ:** |
| PCWriteCond = 1 |
| wr = 0 |
| IRWrite = 0 |
| RegWrite = 0 |
| ALU\_sel = 010 |
| PCSource = 01 |
| ALUSrcA = 1 |
| ALUSrcB = 00 |
| ALUOut\_load = 0 |